Welcome to

30th ANNIVERSARY

DESIGNCON® 2025

WHERE THE CHIP MEETS THE BOARD

Conference

January 28–30, 2025

Santa Clara Convention Center

Expo

January 29–30, 2025

Via Design for 112 Gbps and Beyond: Theory and Reality

Alex Manukovsky, Intel
Yuriy Shlepnev, Simberian Inc.
Joshua Nutzati, Intel
Alexander Kuntsevych, Intel
Itzhak Peleg, Intel
Shimon Mordooch, Intel

Date: Thursday, January 30 • 8:00 AM - 8:45 AM Pacific Time
Location: Ballroom B

OUTLINE

- Introduction
- Bandwidth and Localization
- Design of Vias for Two Stackups
- Reality Check
- New Approach to Viahole Design
- Conclusion

Introduction

- Designing PCB and packaging interconnects for 112-224 Gbps links presents multiple challenges
- Design of vertical transitions, or vias, being one of the most critical elements and **is the main roadblock for 448 Gbps links**
- Vias dissipate and reflect signals, contribute to crosstalk noise through both local and distant coupling
- How to approach the via analysis and design at these data rates?...

State of the Art in Via Analysis

- 3D EM for RL, IL and Local Coupling of Vias
  - FEM – HFSS; FEM + DD – Clarity; BEM - HyperLynx 3D EM; FIT – CST; Simbeor – MoL, TFE;
- 2D EM for Long-Distance Coupling of Vias
  - Physics-based local via model + transmission plane model for PDN
  - Power SI, SI Wave, HyperLynx SI+PI
  - Possible accuracy improvement for some geometries with near-field and far-field separation (validated up to 100 GHz)
- Hybrid 2D + 3D EM – Local and Long-Distance Coupling
  - PEEC, FEM, DGTD,…
  - Still at research stage…

See references and details in the paper…

Via Design Approaches

1) Direct optimization of everything (anti-pads, stitching vias, pads,…) – brute-force approach;
2) Physics-based approach – use of TDR in addition to RL
3) Simultaneous optimization – use of same stackup for multiple layers;
4) Domain decomposition/Zones of control – separate optimization of via sections;`

*A. Carmona-Cruz, K. Scharff, J. Cedeño-Chaves, H. -D. Brüns, R. Rimolo-Donadio and C. Schuster, "Via Transition Optimization Using a **Domain Decomposition** Approach," 2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI), Chambéry, France, 2019, pp. 1-4.*

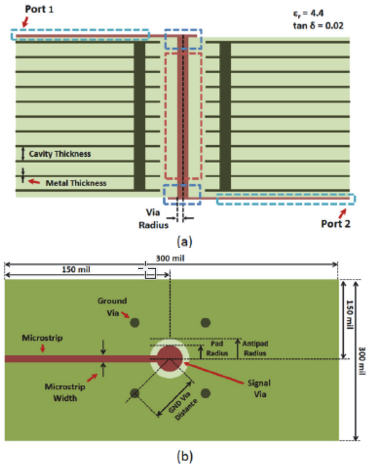
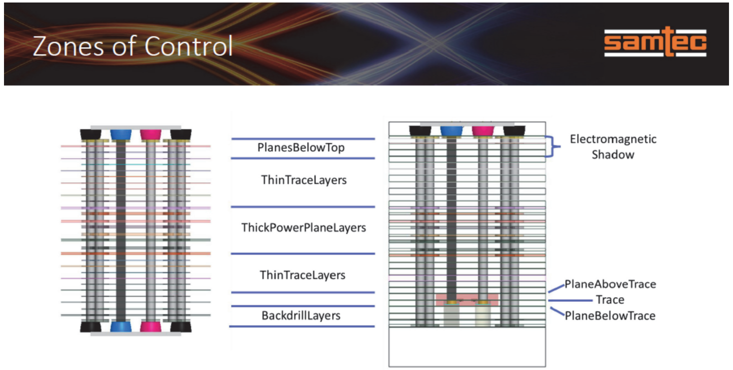


Fig. 1. Signal via in a 11 metal layer PCB with microstrip traces: (a) Side

*S. McMorrow, Breakout Design: Package and Traces, Samtec, gEEk spEEk, 2023 – **zones of control***



*J. Jeon, S. Joshi, D. De Araujo and B. Mutnury, "**Codimensional Optimization** of Differential Via Padstacks," 2022 IEEE 31st Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2022, pp. 1-3.*

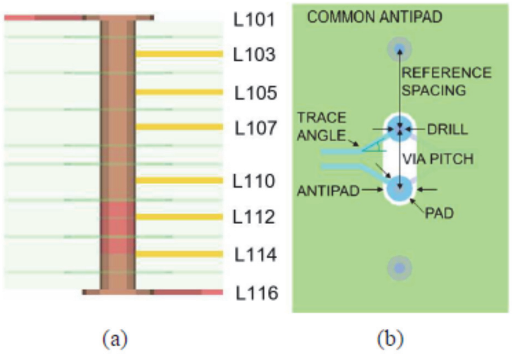


Figure 1. 16 Layer via PCB & Parameters

OUTLINE

- Introduction
- Bandwidth and Localization
- Design of Vias for Two Stackups
- Reality Check
- New Approach to Viahole Design
- Conclusion

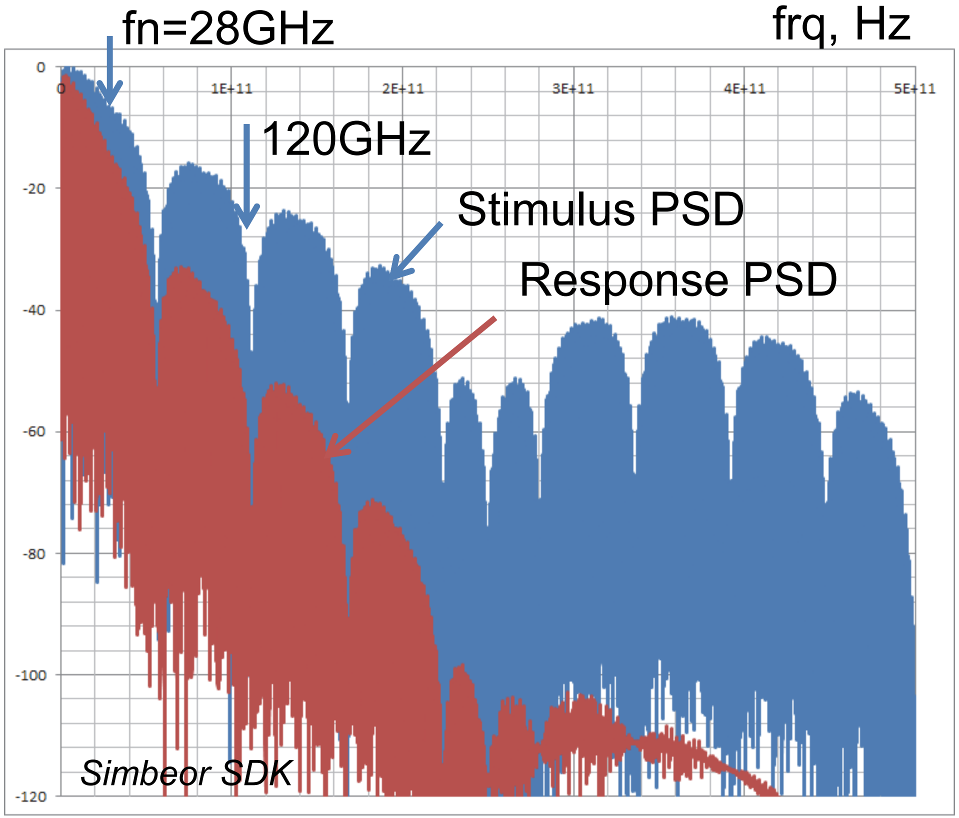
Signal Bandwidth: Power Spectral Density

Example: 112Gbps PAM4, 4ps rise time
10-inch strip line, W=12mil, H=20mil
Meg7 – Wideband Debye: Dk=3.17, LT=0.0011 @ 1 GHz
Copper: RR=1.4, Roughness – Huray- Bracken Model:
SR=0.14 um, RF=8.7

Bandwidth for IL and FEXT depends on link length – the longer the link, the smaller bandwidth may be used
Only 2-3 Nyquist may be required for accurate analysis
Formal pulse analysis can be used for better estimate (*)

Bandwidth for NEXT (crosstalk in vias) is practically the same as the stimulus ☹ - **maximal possible bandwidth must be used**

(*) *Y. Shlepnev, How Interconnects Work:* ***Bandwidth for Modeling and Measurements****, Signal Integrity Journal, April 12, 2022*



Coupling and Dissipation in Balance of Power

$$\boldsymbol{P_{out} = P_{in} - P_{reflected} - P_{dissipated} - P_{leaked} + P_{coupled}}$$

$\boldsymbol{P_{dissipated}}$ includes energy absorbed by materials ($\boldsymbol{P_{absMat}}$) and by boundary conditions ($\boldsymbol{P_{absBC}}$)

$$\boldsymbol{P_{dissipated} = P_{absMat} + P_{absBC}}$$

$$P_{in} = |a_1|^2\ [Wt], a_2 = 0$$

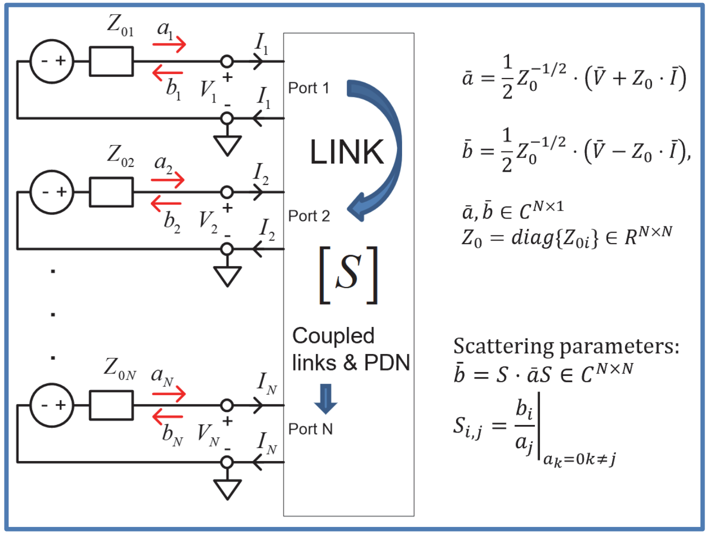
$$P_{out} = \left|S_{2,1}\right|^2 P_{in}$$

$$P_{reflected} = \left|S_{1,1}\right|^2 P_{in}$$

$$\boldsymbol{P_{dissipated} = \left(1 - \sum_k \left|S_{k,1}\right|^2\right) P_{in}}$$

$$P_{leaked} = \left(\sum_{k\neq 1,2} \left|S_{k,1}\right|^2\right) P_{in}$$

$$\boldsymbol{P_{coupled} = \sum_{k\neq 1,2} \left|S_{2,k}\right|^2 P_{ink}}$$



1. Can $\boldsymbol{P_{coupled}}$ be evaluated in isolation with PML boundary conditions (BC)?

2. Can $\boldsymbol{P_{dissipated}}$ evaluated for via isolated with PML BC be used as a metric of via localization and possible coupling?

(*)Y. Shlepnev, How Interconnects Work: ***Reflections from Discontinuities*** *, Simberian App Note #2022_01, January 10, 2022.*

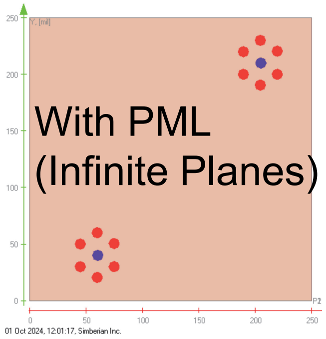
Single-Ended Vias Coupling and Localization

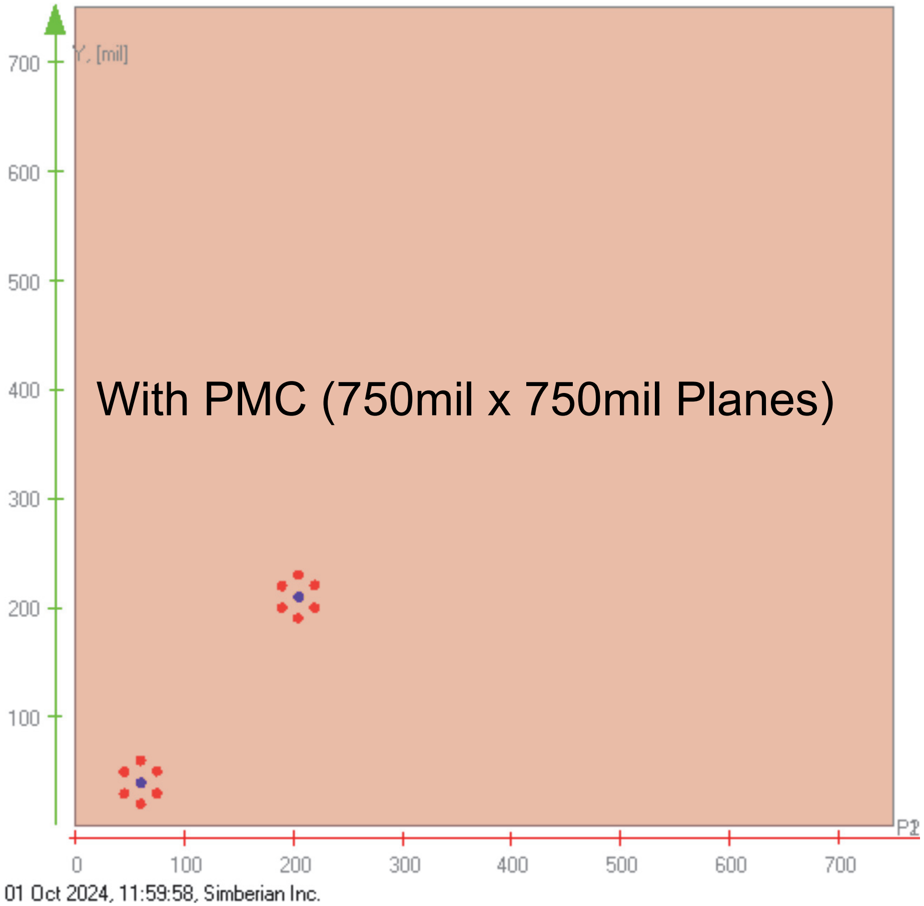
Two 0.77mil copper planes, separated by dielectric with Dk=3, LT=0.001

Two signal vias at 220mil (10mil diameter)
Number of stitching vias (Nstv) from 0 to 6 at about 20mil distance from signal

4-port structure with 50Ohm terminations

Physics-based model with 2D analysis in Simbeor 3DTF solver





SE Via Coupling – Plane Separation H=9mil

Coupling is reduced by increase of Nstv

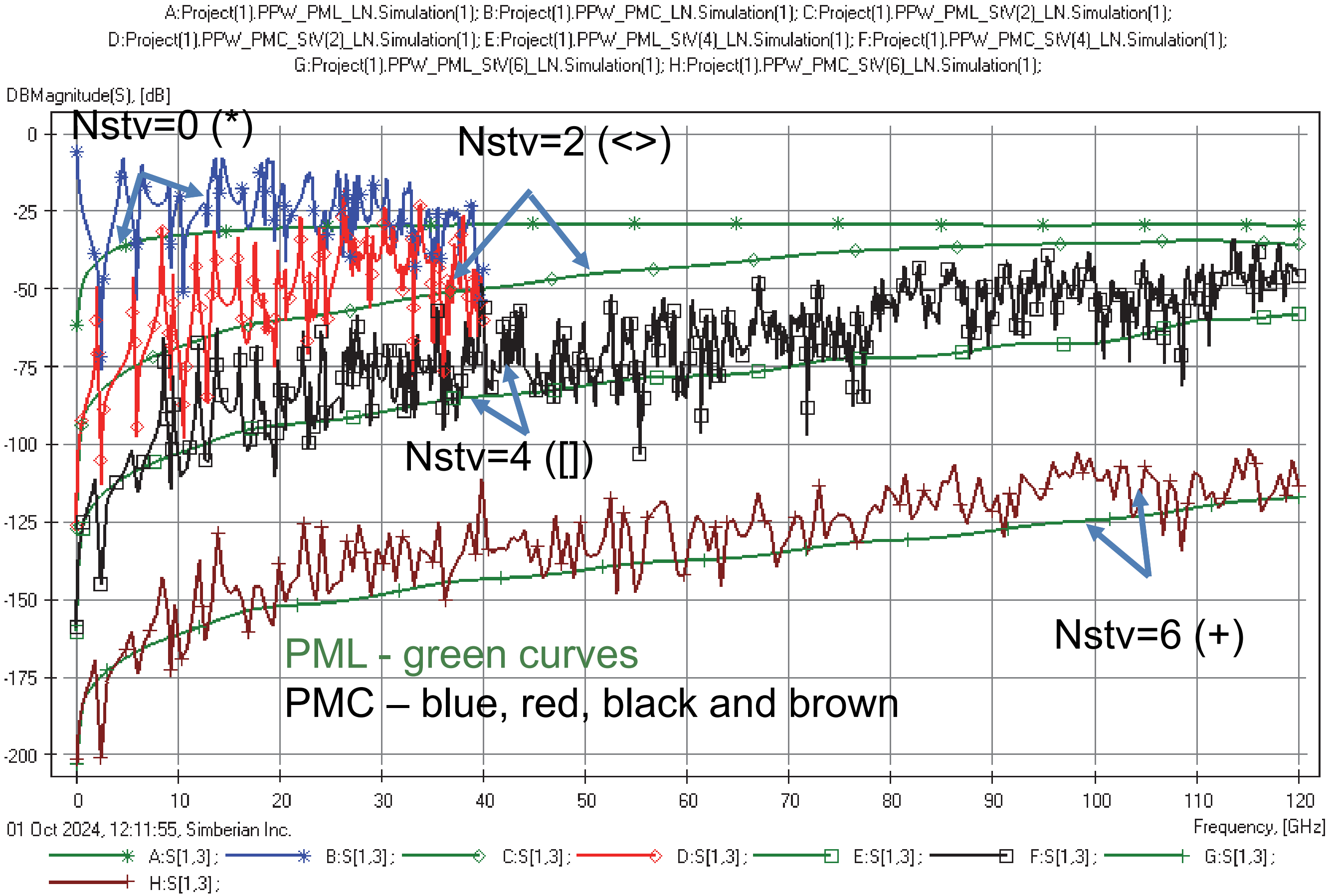
Resonances in PPW affect coupling

Coupling saturates as frequency increases (remarkable)

Coupling increases with plane separation (see Appendix)

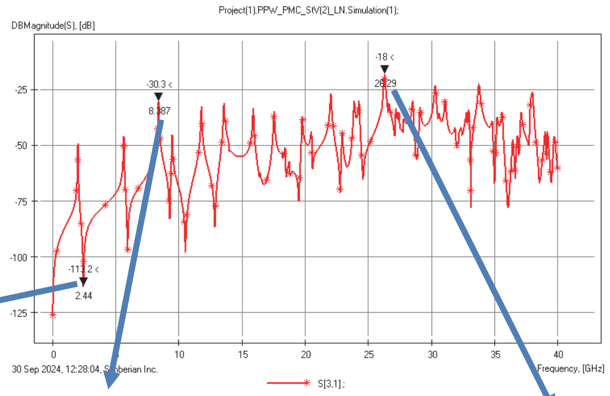
2 or 4 stitching vias may be not enough for extended bandwidth

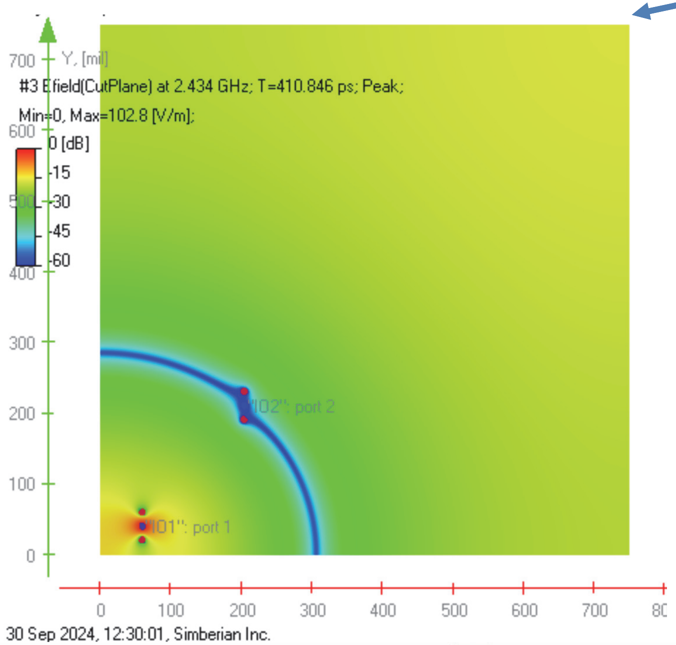
Realistic analysis has enormous complexity due to resonances

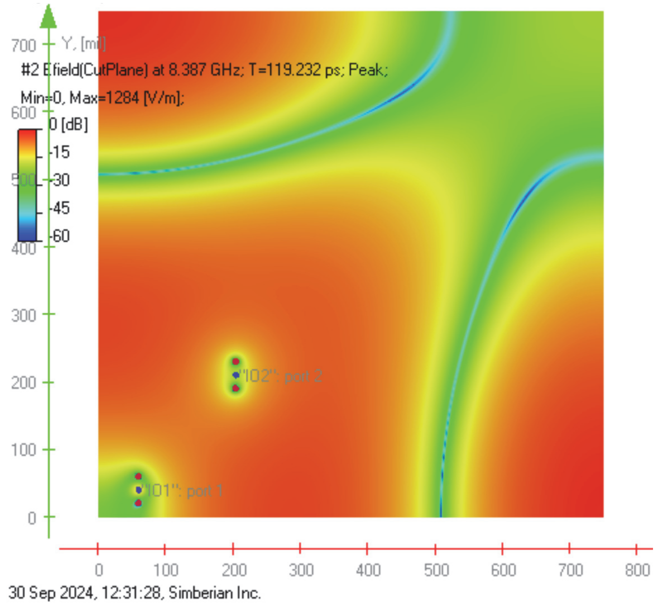


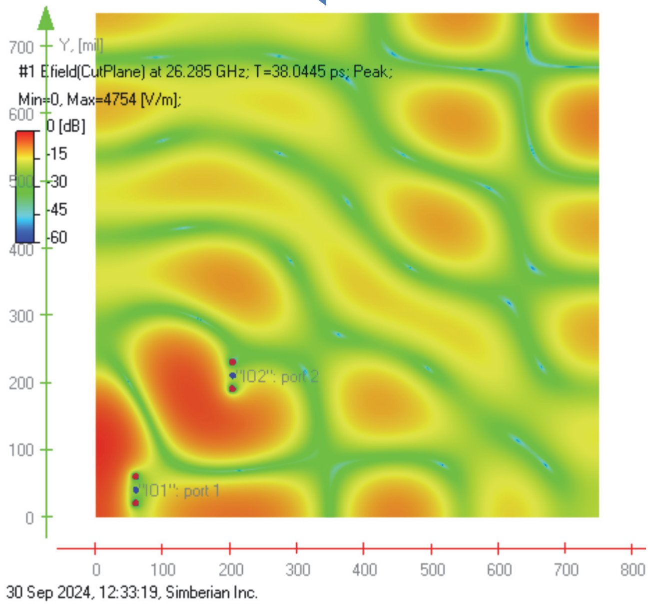
PPW Resonances: H=9mil

750mil x 750mil with PMC, Nstv=2
Electric field with 0.5V excitation at corner via
Minima and maxima depends on PDN geometry and all terminations – difficult to account for realistic design





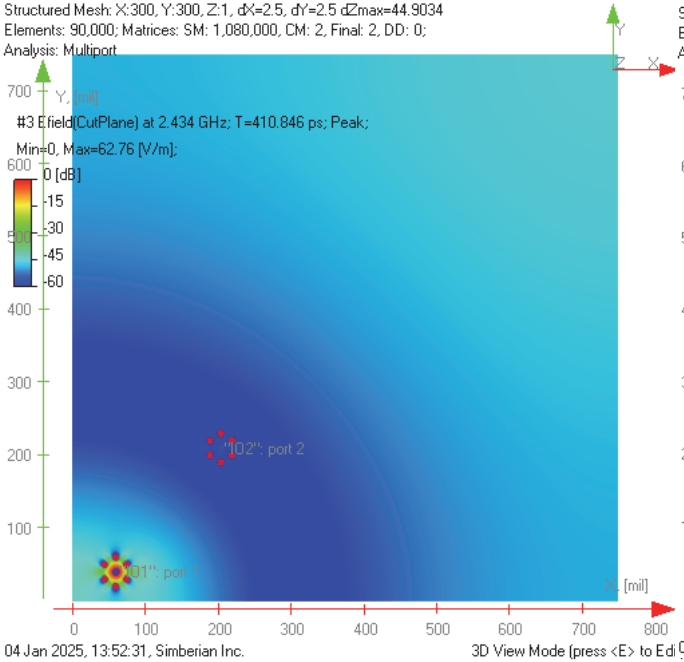


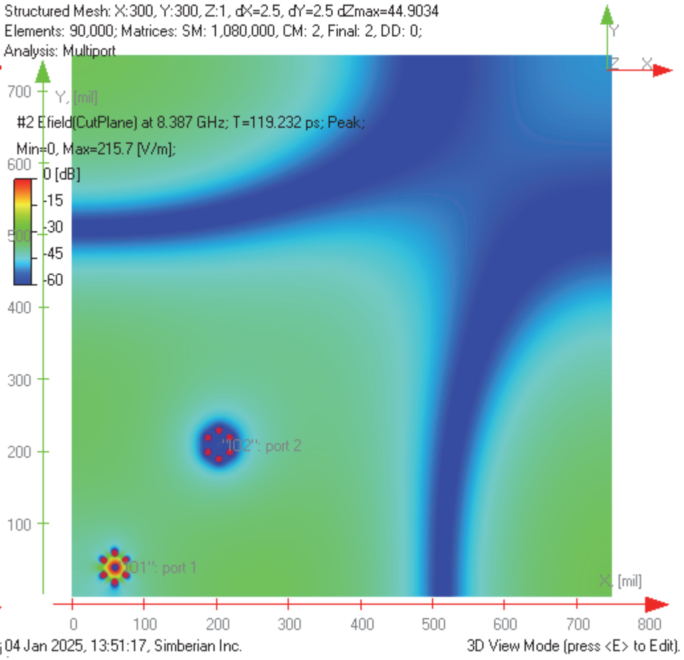


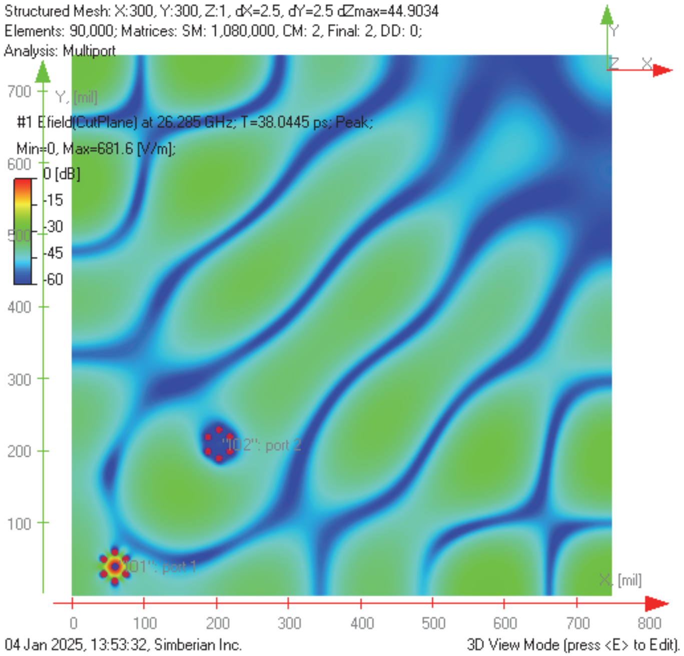
Coupling Reduction: H=9mil

750mil x 750mil with PMC, Nstv=6
Electric field with 0.5V excitation at corner via
No need to simulate the whole board

Coupling is not sensitive to distance – defined mostly by maxima and minima or PP resonances
Coupling increased with the number of parallel planes and with the number of aggressors (see Appendix)







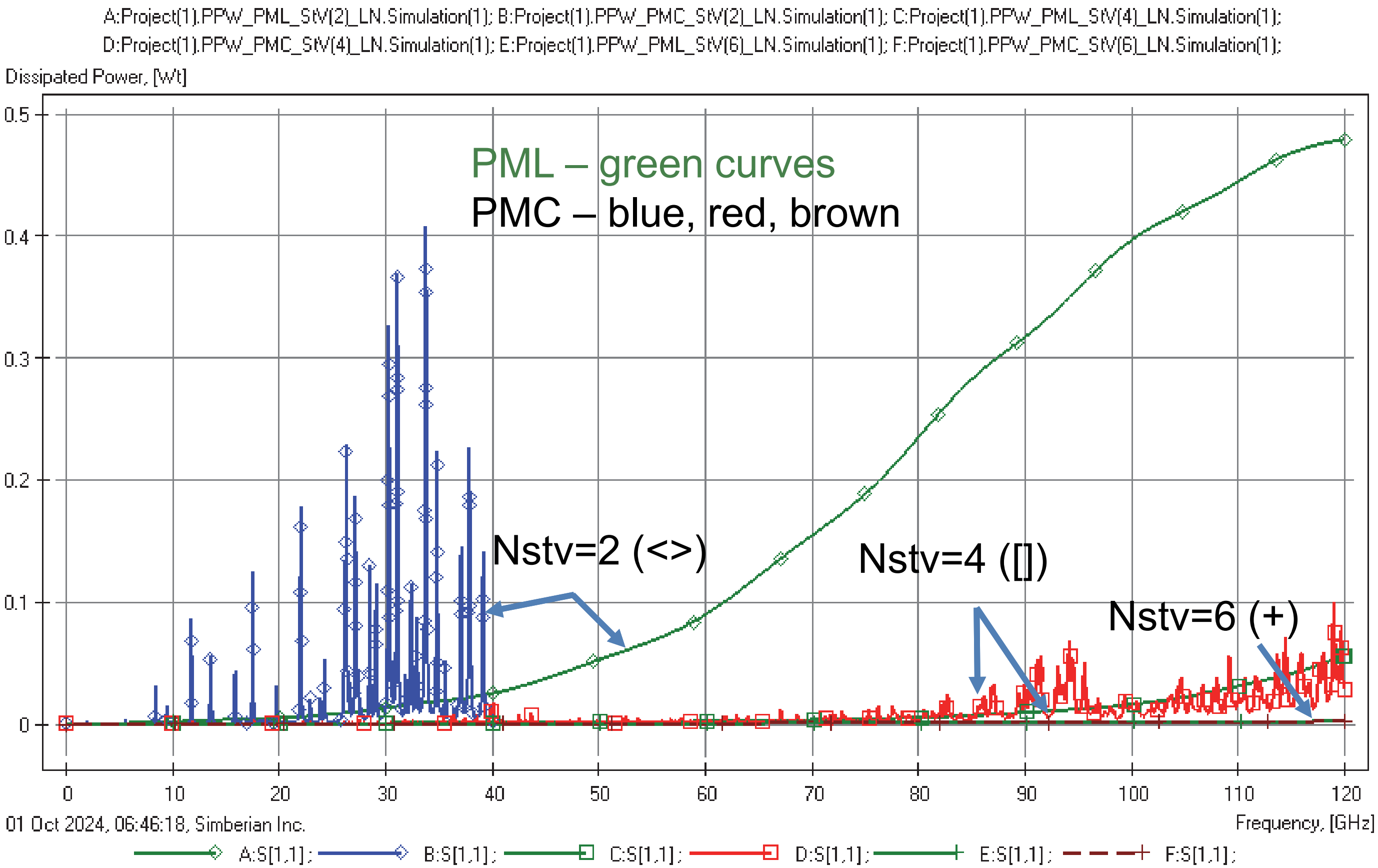
SE Via Dissipated Power and Stitching (H=9mil)

$$P_{dissipated} = \left(1 - \sum_k \left|S_{k,1}\right|^2\right) P_{in}$$

Excitation: 1 Wt

Stitching vias reduce power dissipation (leaks)

Power dissipation for sufficiently localized structures can be evaluated with PML boundaries (infinite planes)



SE Via Dissipated Power – 3D EM Model

$$P_{dissipated} = \left(1 - \sum_k |S_{k,1}|^2\right) P_{in}$$

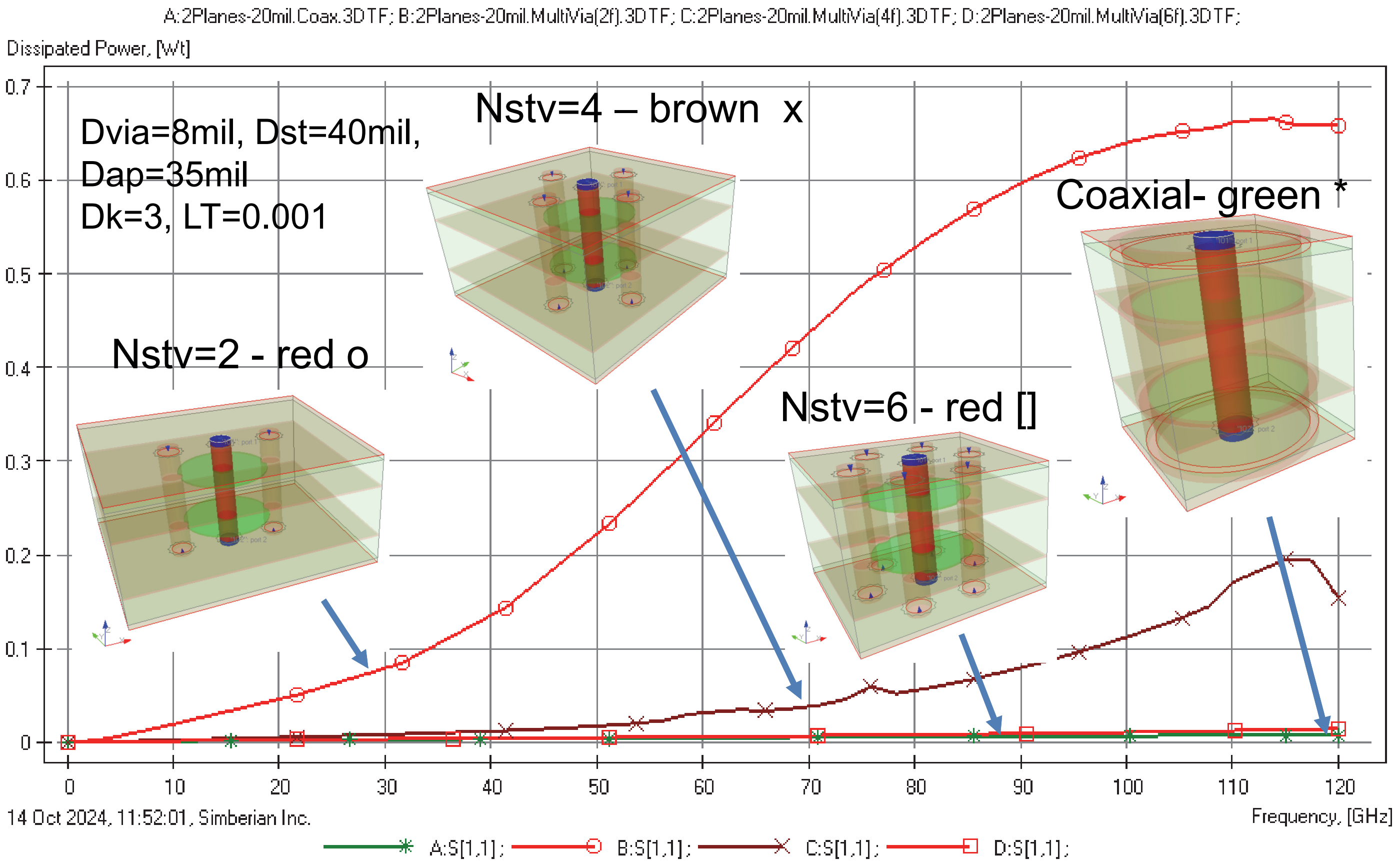
3D EM model for estimation of dissipated power and comparative analysis

2 Planes, H=20mil

Excitation: 1 Wt

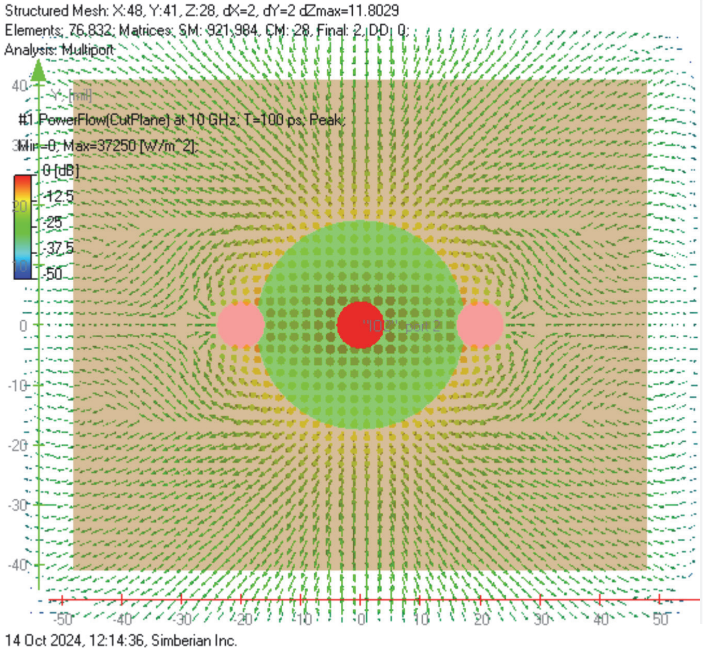
Stitching vias reduce dissipated power and potential coupling

Simbeor 3DTF, PML



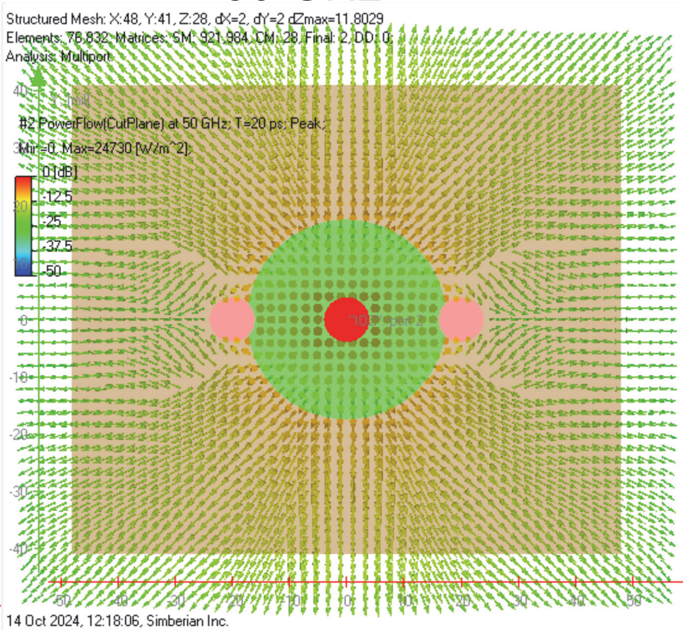
SE Via Power Flow Density, Nstv=2

10 GHz



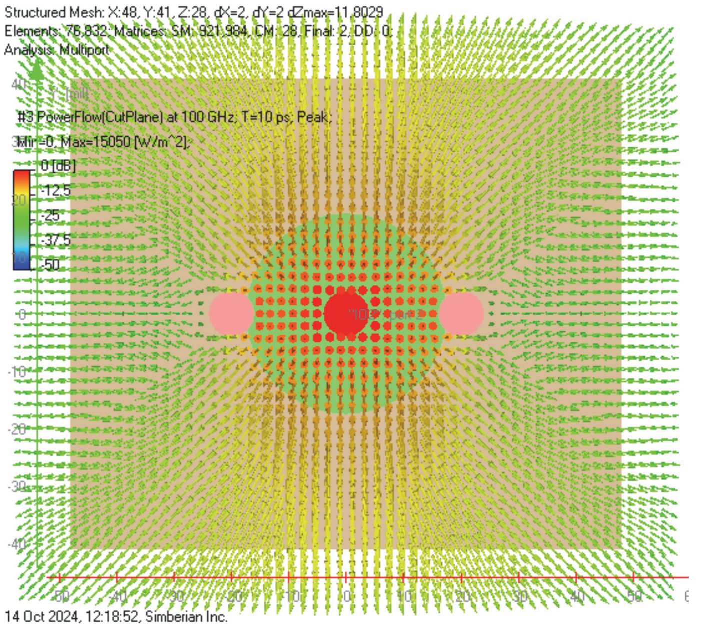
DP=2%

50 GHz



DP=22%

100 GHz

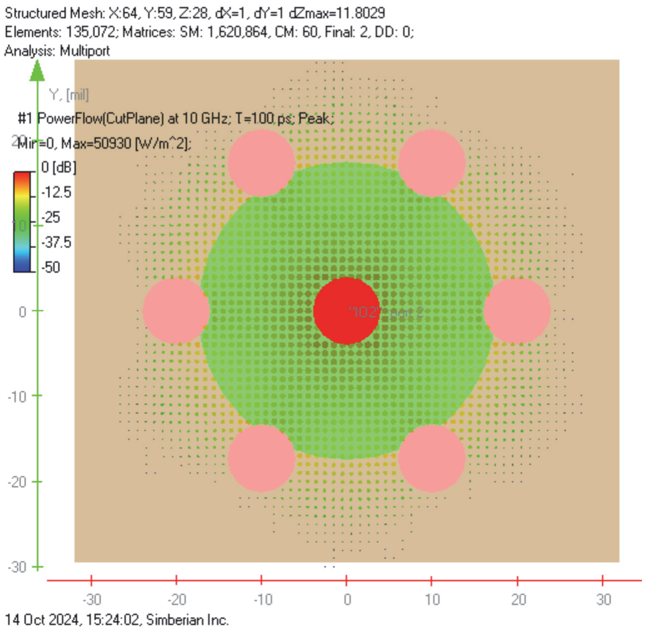


DP=64%

Peak PFD, Simbeor 3DTF, PML BC, Dvia=8mil, Dst=40mil, Dap=35mil, Dk=3, LT=0.001

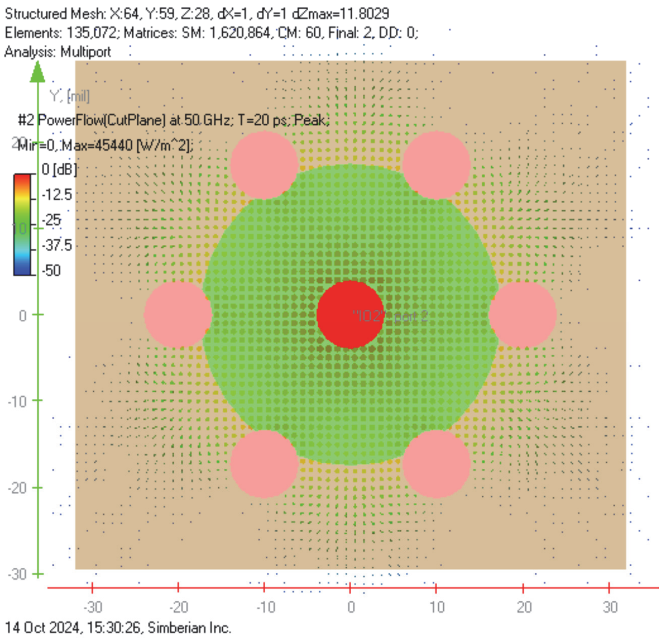
SE Via Power Flow Density, Nstv=6

10 GHz



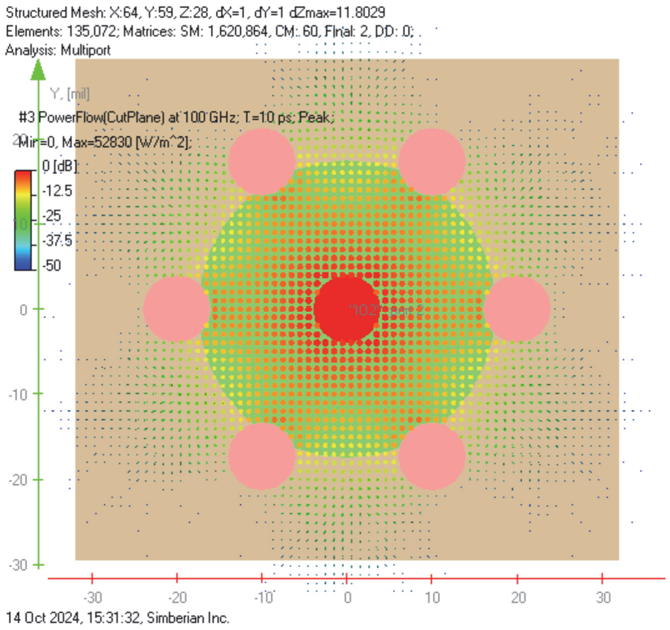
DP=0.15%

50 GHz



DP=0.46%

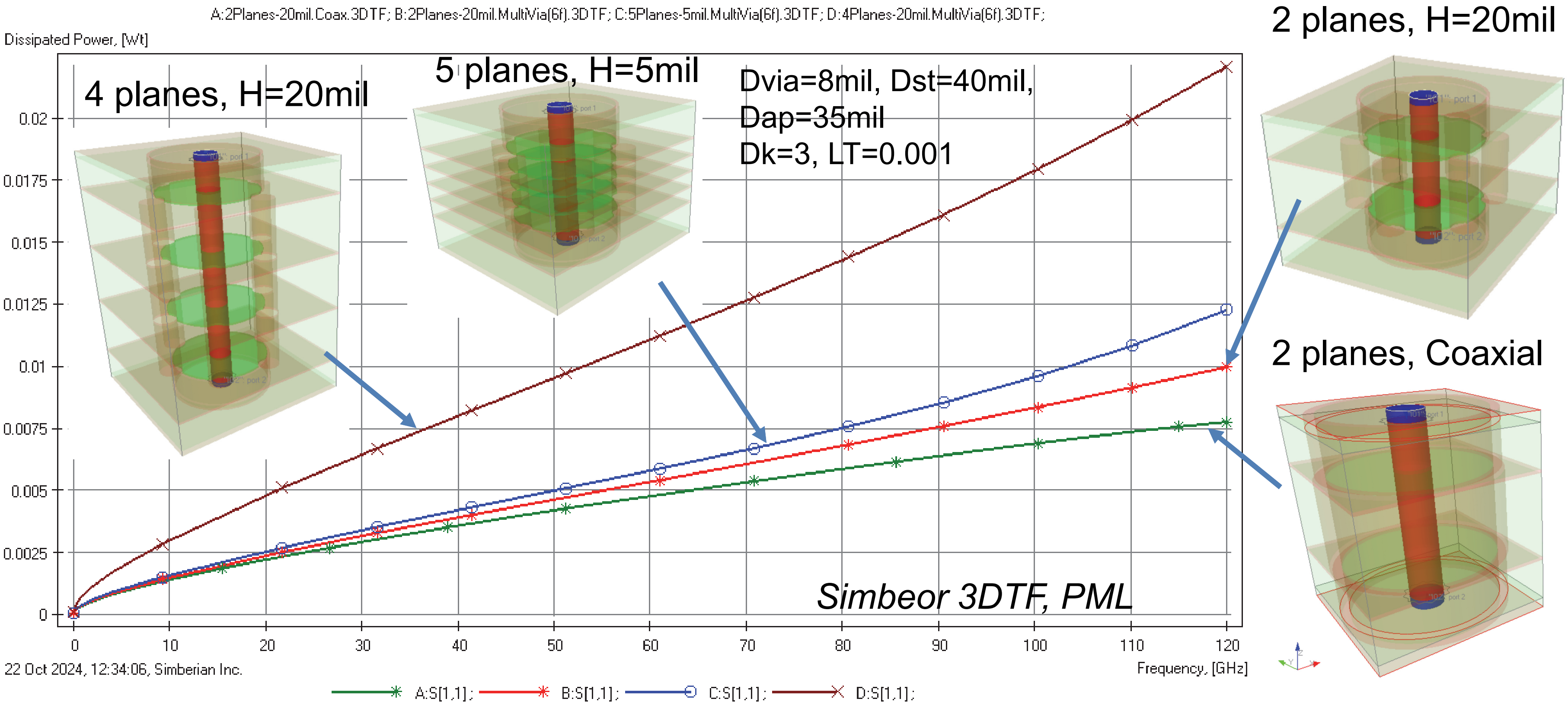
100 GHz



DP=0.8%

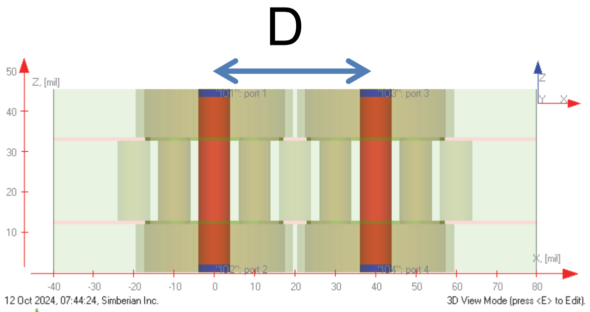
Peak PFD, Simbeor 3DTF, PML BC, Dvia=8mil, Dst=40mil, Dap=35mil, Dk=3, LT=0.001

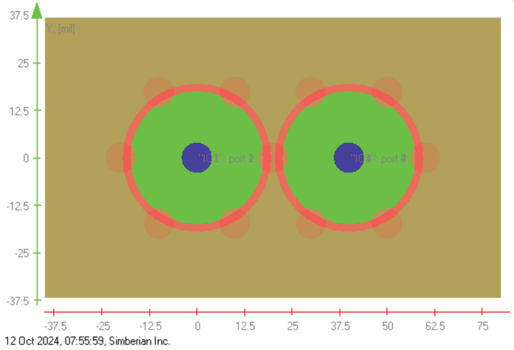
SE Vias Dissipated Power, Nstv=6



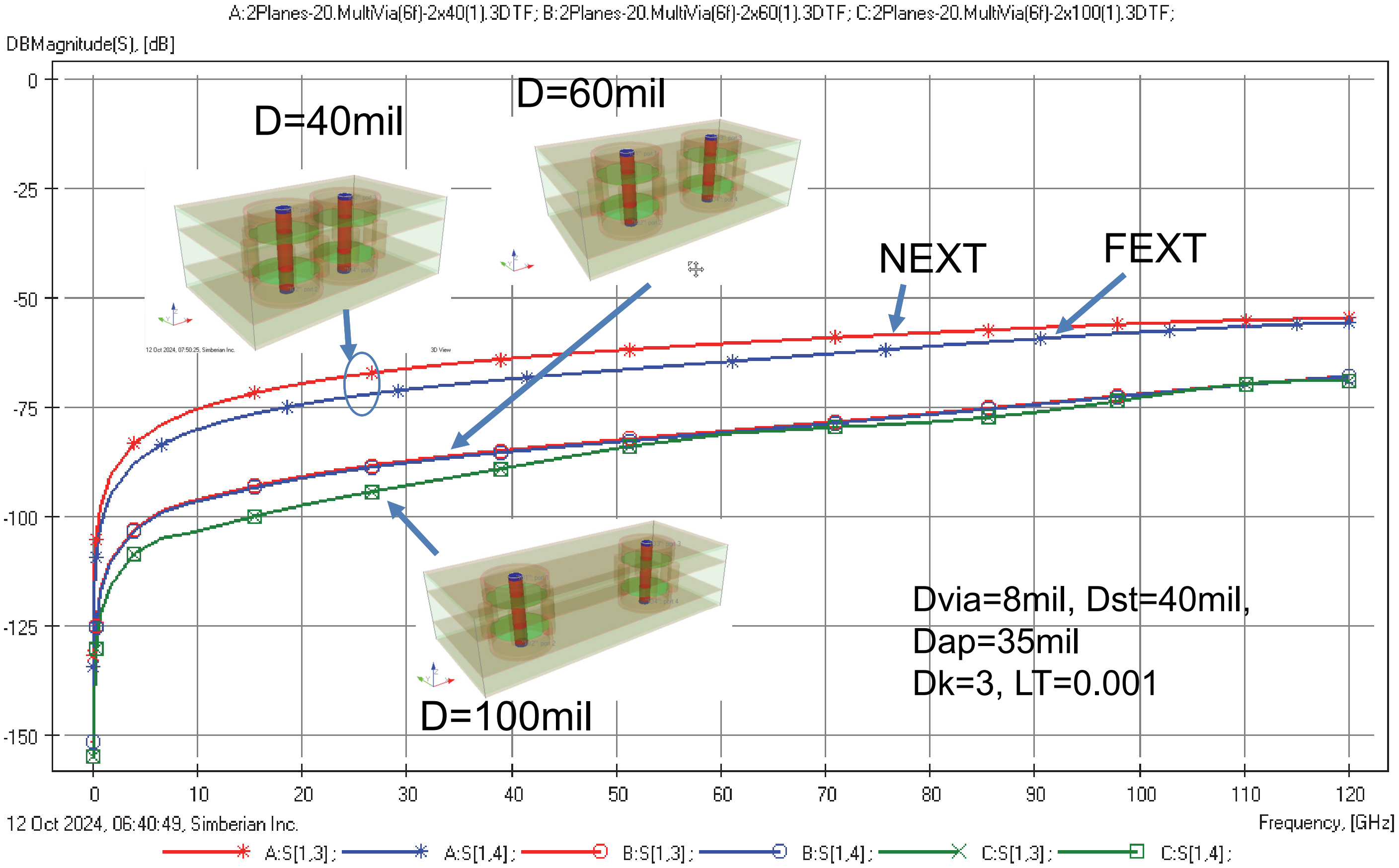
DP increases with number of layers NL (proportional to NL) and decrease with smaller separation H

SE Vias Local Coupling – 2 planes, H=20 mil





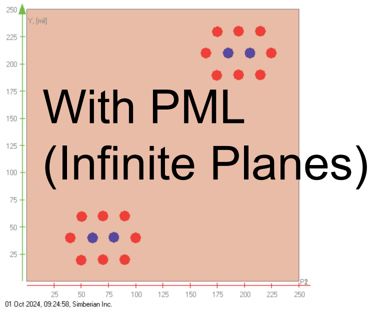
Dvia=8mil, Nstv=6, Dk=3, LT=0.001
Dst=40, Dap=35
Simbeor 3DTF, PML
See other cases in Appendix

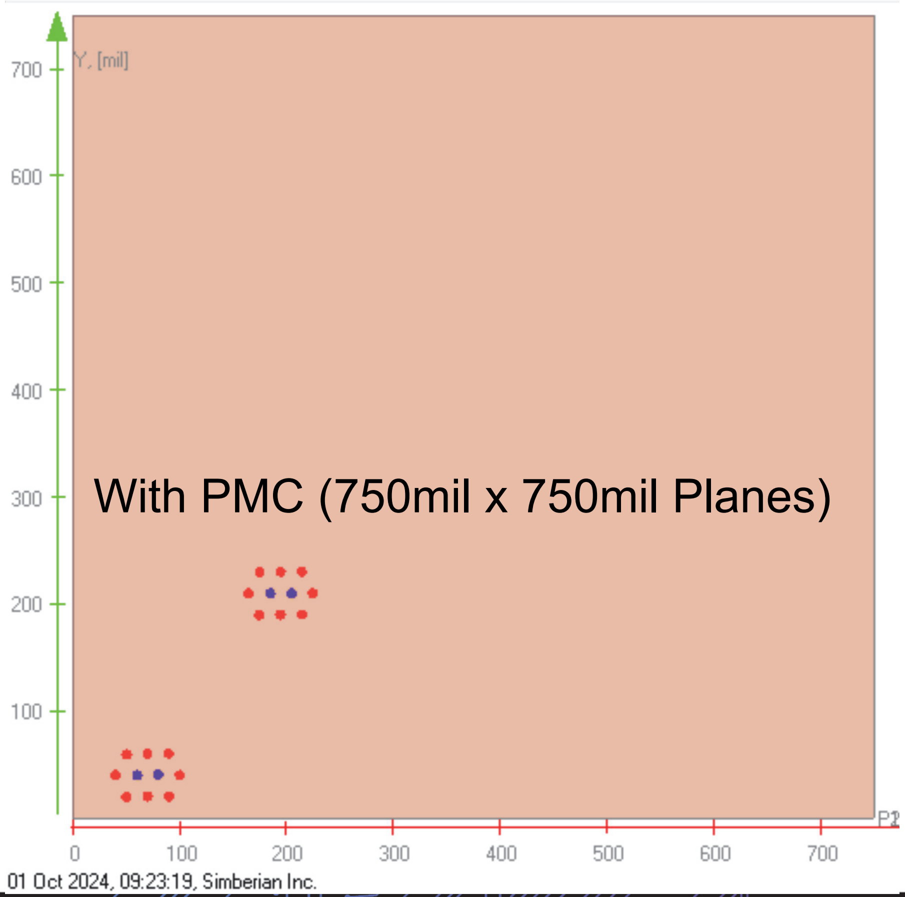


Diff. Vias Localization and Distant Coupling

Two 0.77mil copper planes, separated by 9mil dielectric with Dk=3, LT=0.001
Differential signal vias 20mil distance (10mil diameter), two pairs at ~220mil
Number of stitching vias (Nstv) from 0 to 8 at about 20mil distance from signal
8-port structure with 50Ohm terminations

Physics-based model with 2D analysis in Simbeor 3DTF solver





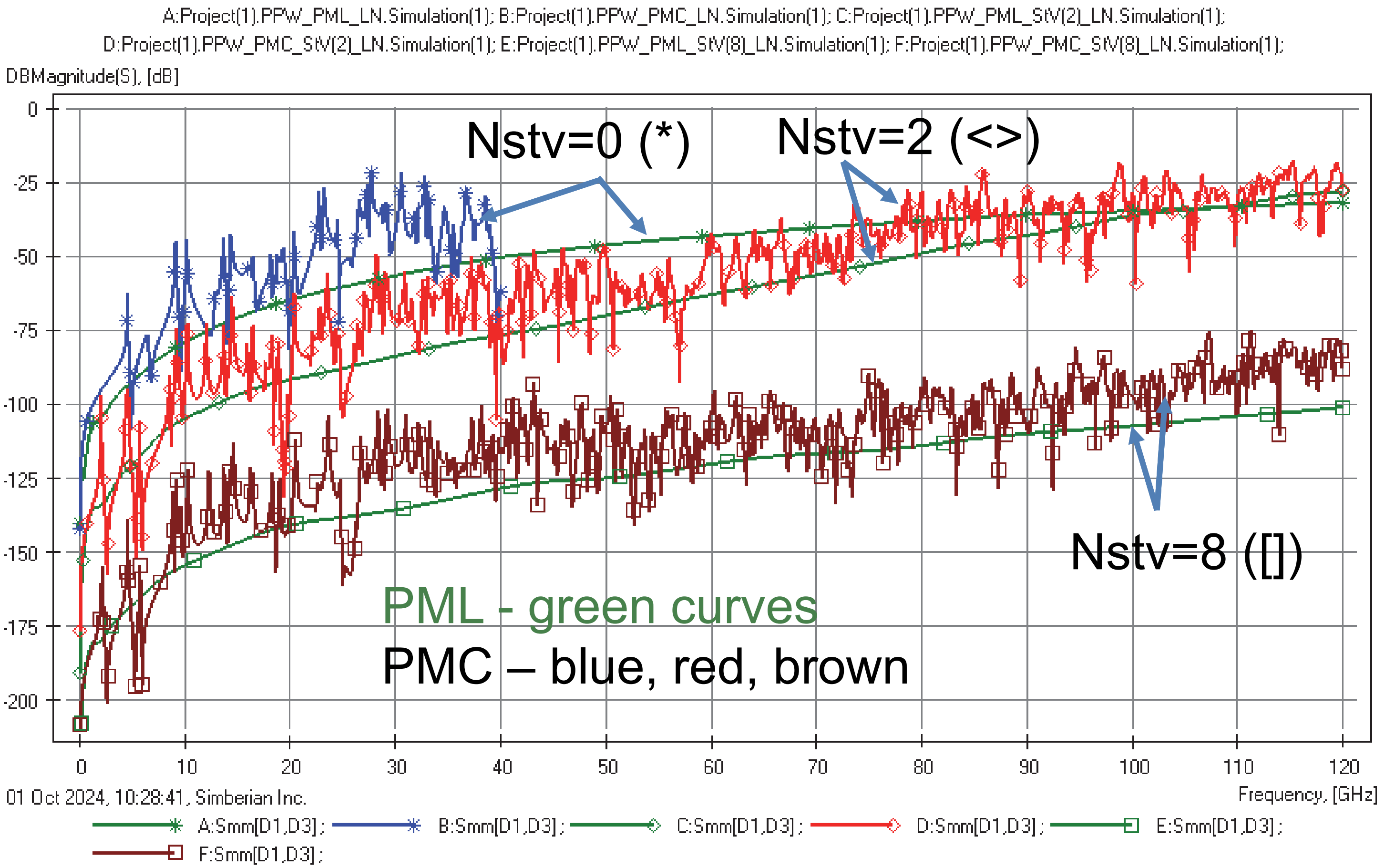
Differential Mode Coupling

DM coupling is reduced by increase of Nstv

Two stitching vias may be not enough for extended bandwidth

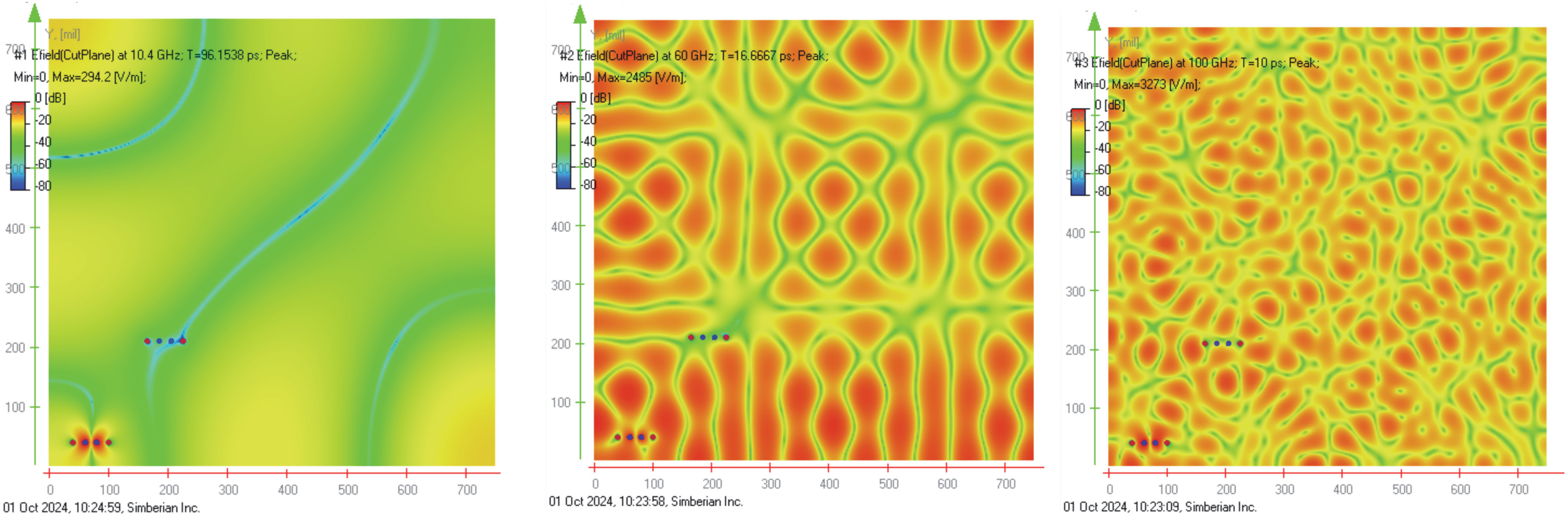
Common mode coupling is much worse (similar to SE) In addition, there is substantial **common to differential mode conversion**

See more in Appendix



Coupling and Mode Conversion – Fields

750mil x 750mil with PMC, Nstv=6
Electric field for 1V differential source at corner vias
Difficult to account in 3D EM analysis

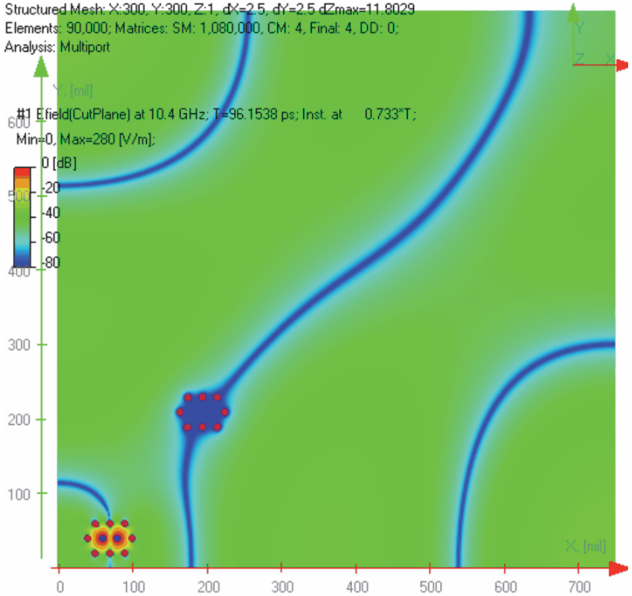


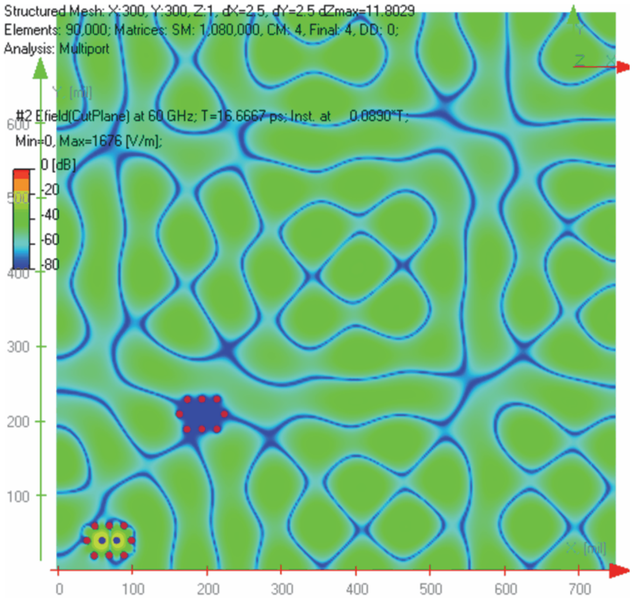
Coupling Reduction with Stitching Vias

750mil x 750mil with PMC, Nstv=8

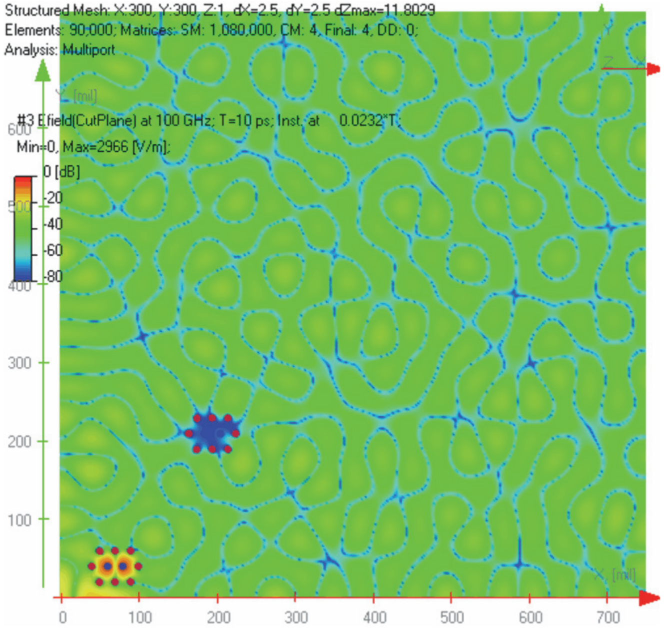
Electric field for 1V differential source at corner vias

Does not need 3D EM analysis of whole boards





(animated)

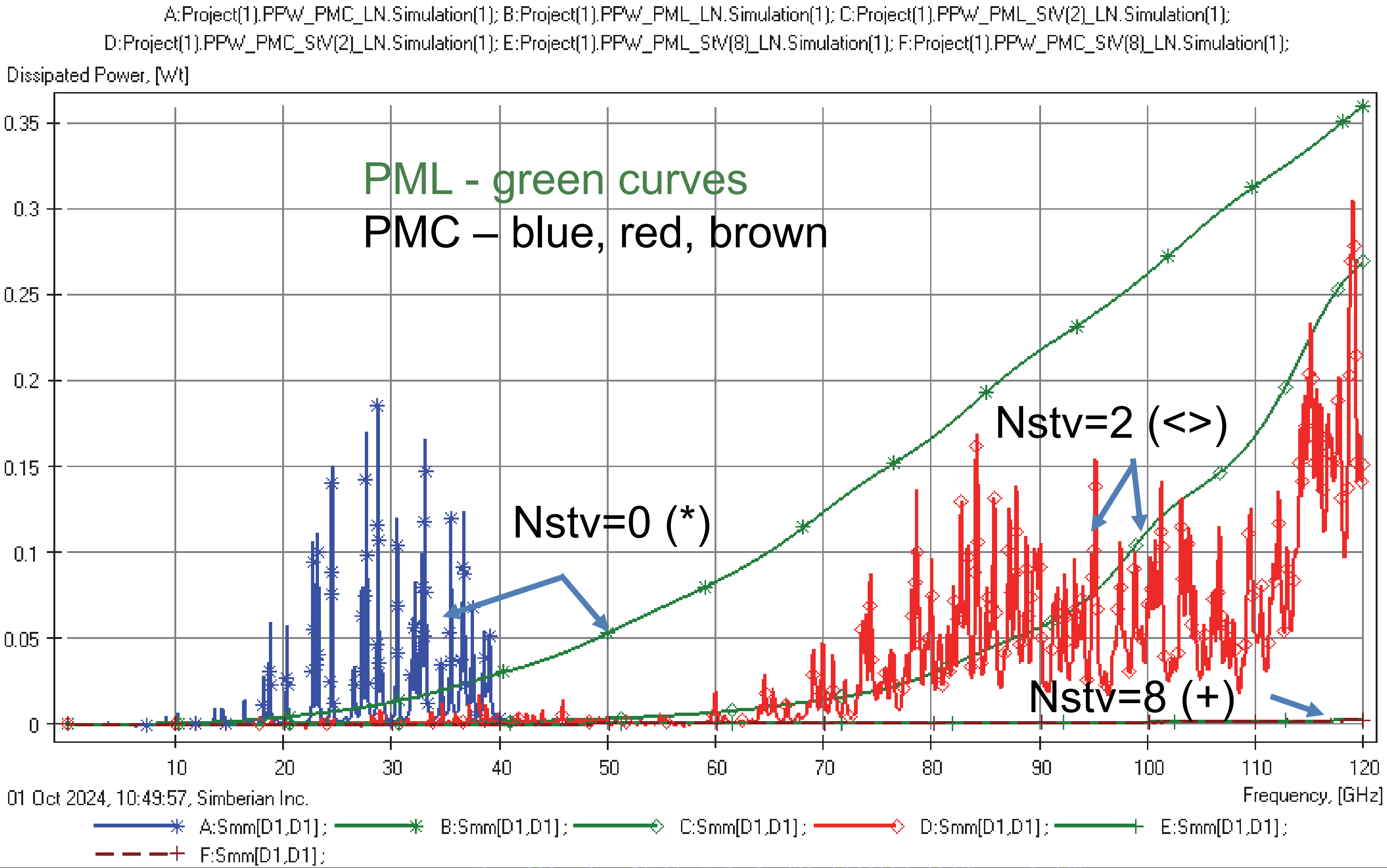


Differential Mode Dissipated Power

$$P_{dissipated} = \left(1 - \sum_k |S_{k,1}|^2\right) P_{in}$$

Stitching vias reduce power dissipation (leaks)

Power dissipation for sufficiently localized structures can be evaluated with PML boundaries (infinite planes)



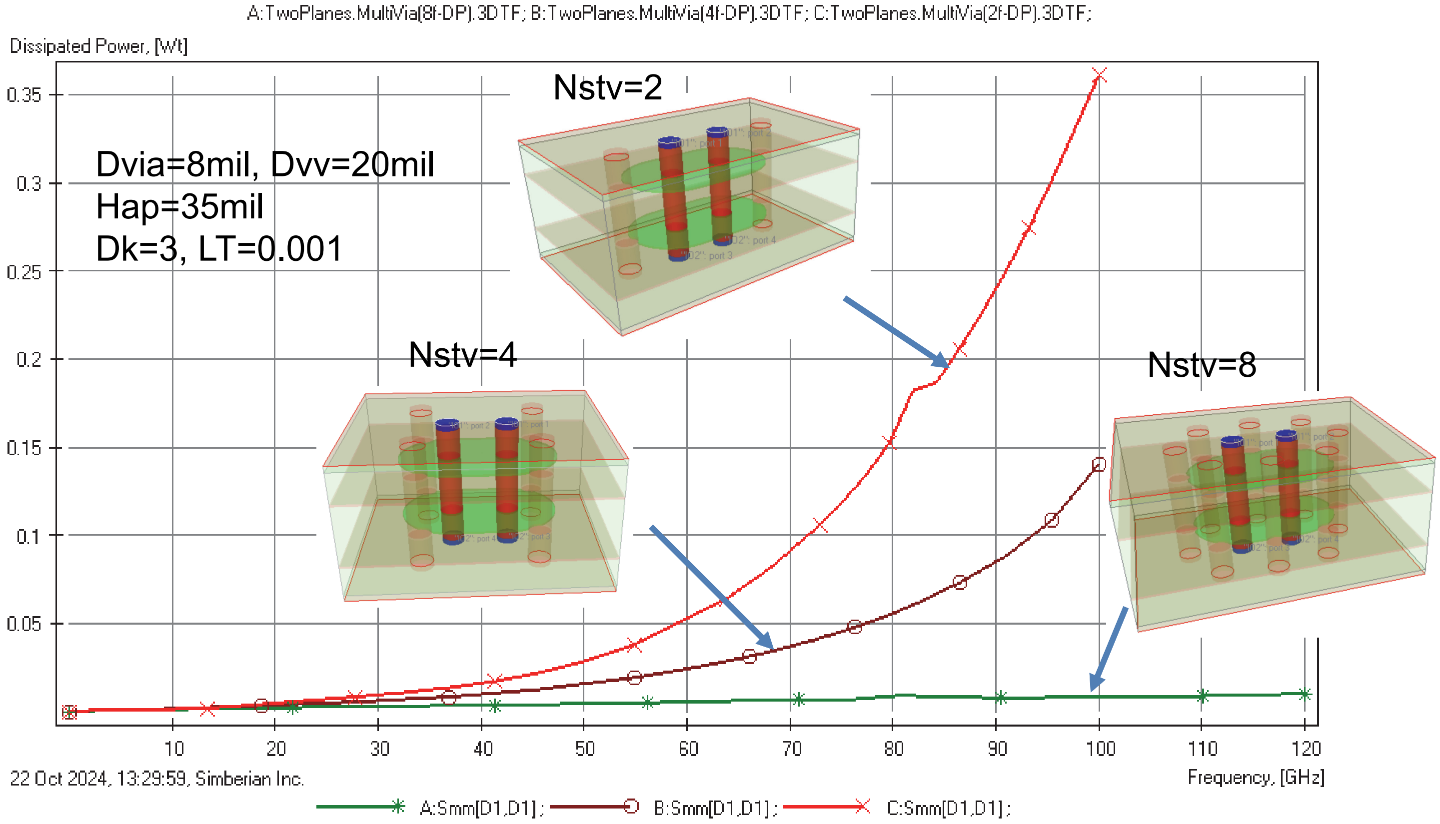
Differential Vias – Dissipated Power, 3D EM

$$P_{dissipated} = \left(1 - \sum_k \left|S_{k,1}\right|^2\right) P_{in}$$

Diff. Excitation 1 Wt

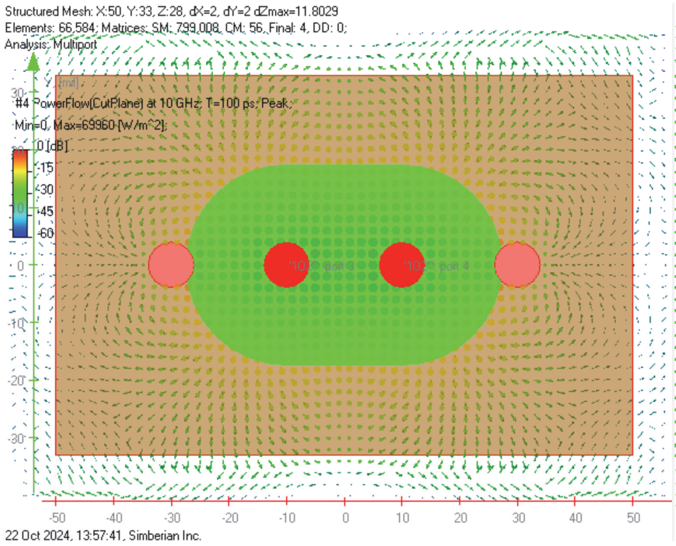
Stitching vias reduce dissipated power and possible leaks and coupling

Simbeor 3DTF, PML



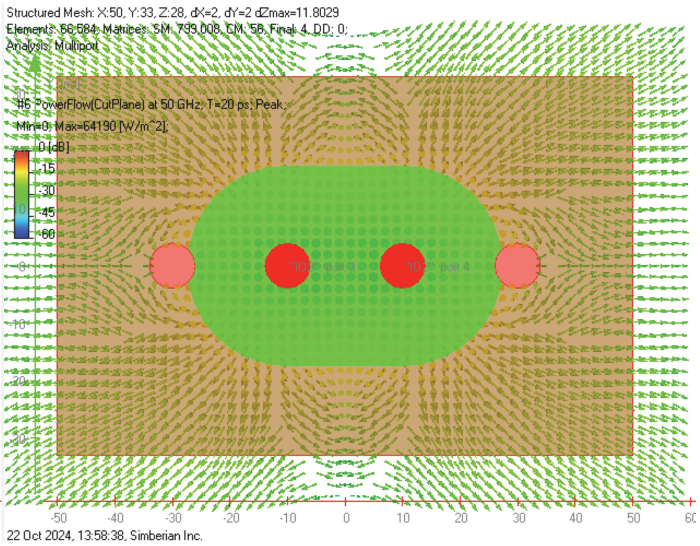
Diff. Vias Power Flow Density, Nstv=2

10 GHz



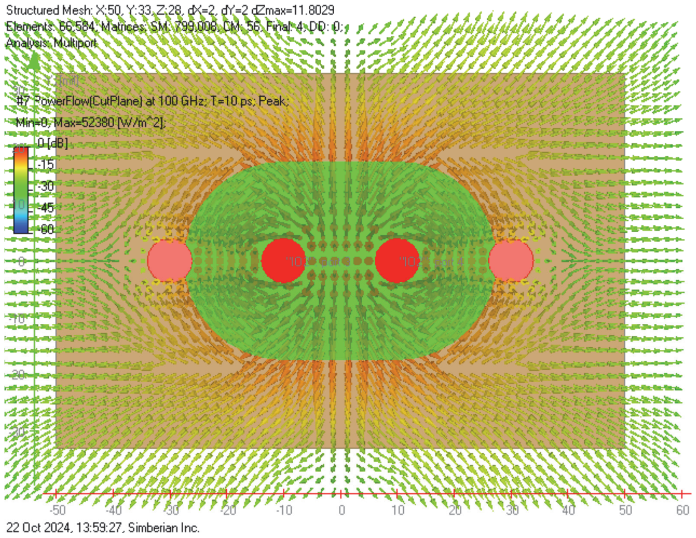
DP=0.12%

50 GHz



DP=2.9%

100 GHz

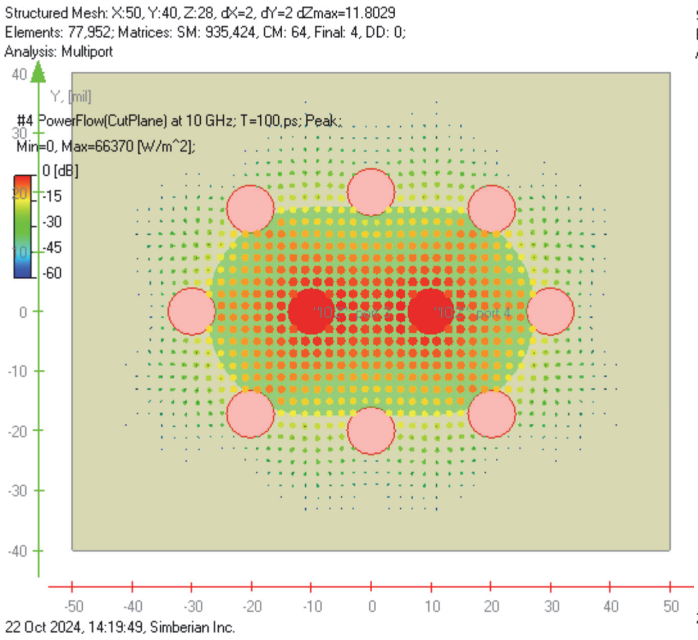


DP=36%

Peak PFD, Simbeor 3DTF, PML BC, Dvia=8mil, Dvv=20mil, Hap=35mil, Dk=3, LT=0.001

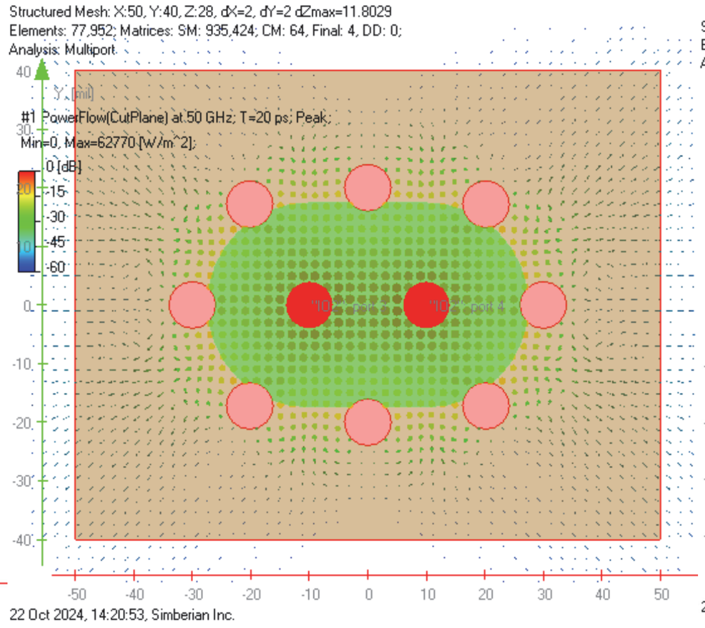
Diff. Vias Power Flow Density, Nstv=8

10 GHz



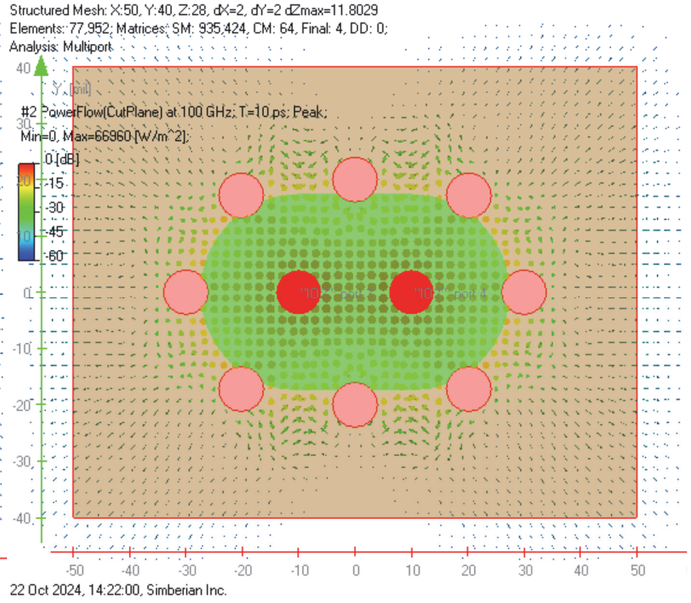
DP=0.13%

50 GHz



DP=0.45%

100 GHz



DP=0.84%

Peak PFD, Simbeor 3DTF, PML BC, Dvia=8mil, Dvv=20mil, Hstv=40mil, Hap=35mil, Dk=3, LT=0.001

Summary on Localization

- Stitching vias reduce coupling
  - Suppress effect of resonances in PDN
  - PML BC can be used to evaluate possible coupling
- Stitching vias reduce dissipated power
  - Dissipated power (DP) can be used as a comparative measure of isolation
  - Sufficiently localized vias can be simulated in isolation
- Stitching vias reduce dependency of RL/IL on PDN geometry (see Appendix)
- **Stitching vias enable analysis of vias in isolation with any boundary conditions**

Localize or Face Uncertainties…

Localization Frequency

Frequency

Localized	Non-Localized
Predictable with analysis in isolation	Requires analysis with PDNs
Any boundary conditions can be used for analysis in isolation	Low-impedance ABC are required for simulation in isolation
Local coupling can be included	Hybrid 2D+3D analysis is required
EASY	DIFFICULT

Localization of any via breaks as frequency grow…

Use Dissipated Power as the localization metric

More on localization and crosstalk in Y. Shlepnev, Tutorial – How Interconnects Work: Crosstalk Anatomy & Quantification, Tuesday, DesignCon 2025, January 28.

OUTLINE

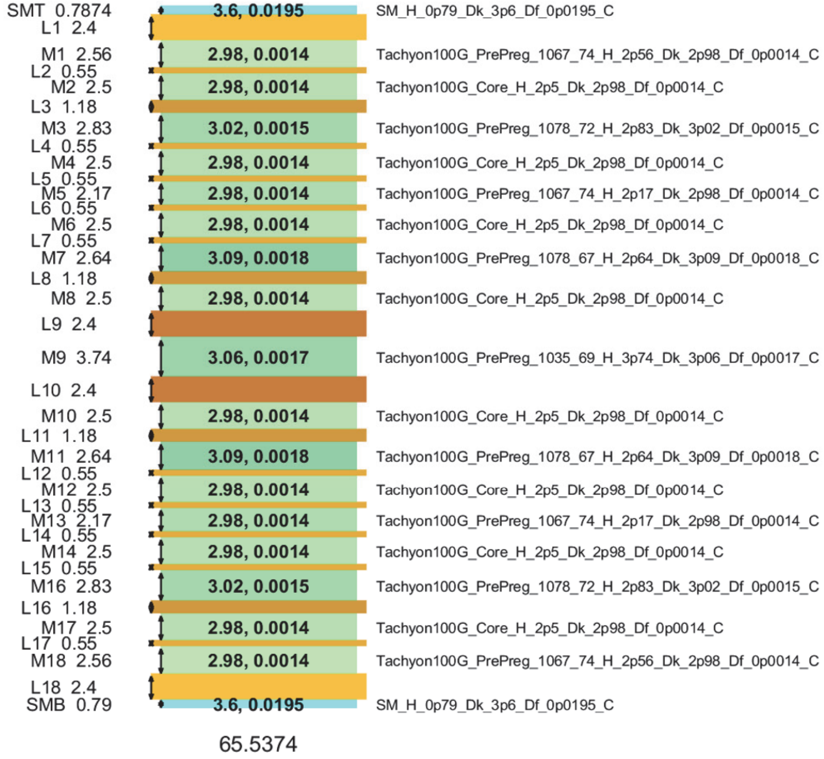
- Introduction
- Bandwidth and Localization
- Design of Vias for Two Stackups
- Reality Check
- New Approach to Viahole Design
- Conclusion

Initial Design Approach for 112Gbps PAM4 Links

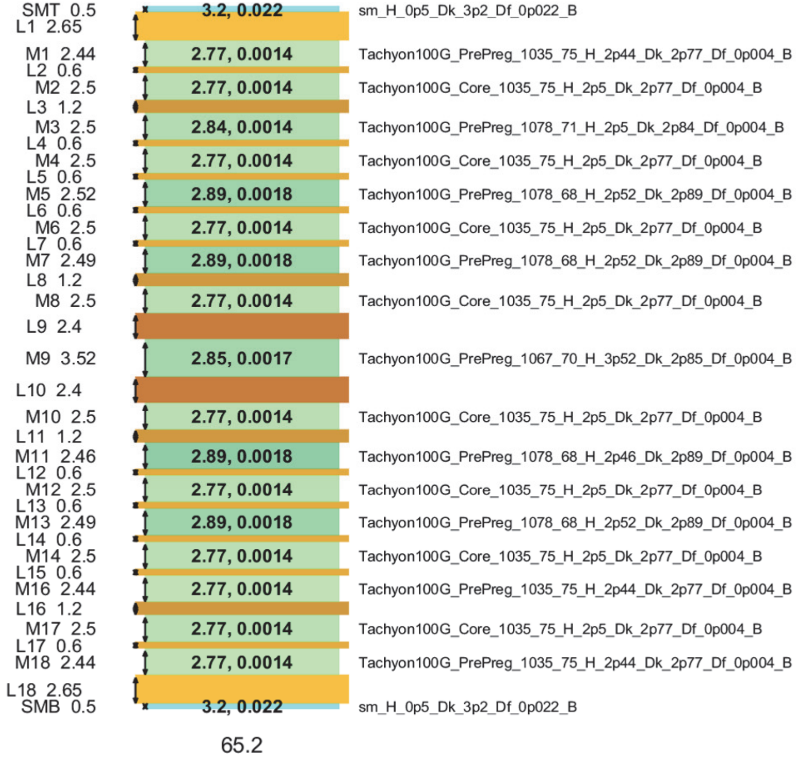
- **Goals:**
  - Ensure **localization** up to 2xNyquist (56GHz)
  - Make sure that reflection are below target defined with polyline
  - Use one via layout for two similar stackups
- **Process:**
  - Build solution space with possible vias geometries **satisfying reflection criteria simultaneously for two stackups**
  - Each configuration is ranked by the distance from the reflection target – the lower the reflection over the bandwidth of the signal, the higher the score
  - Via with the highest score for two stackup modifications is selected for the production

18 Layer Similar Stackups

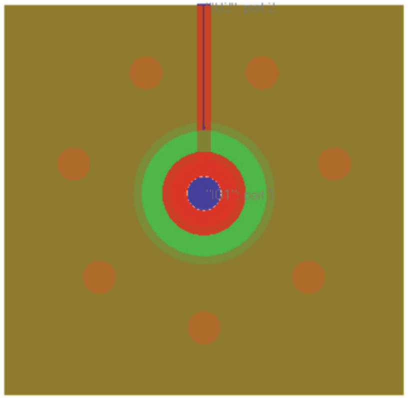
Stackup 1

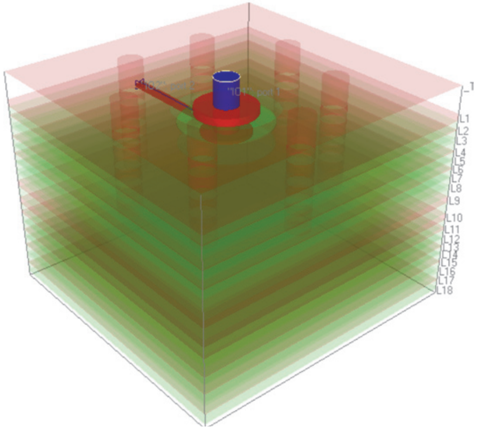


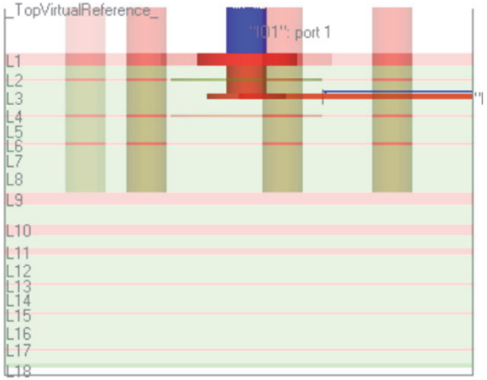
Stackup 2



Best Configurations for L3





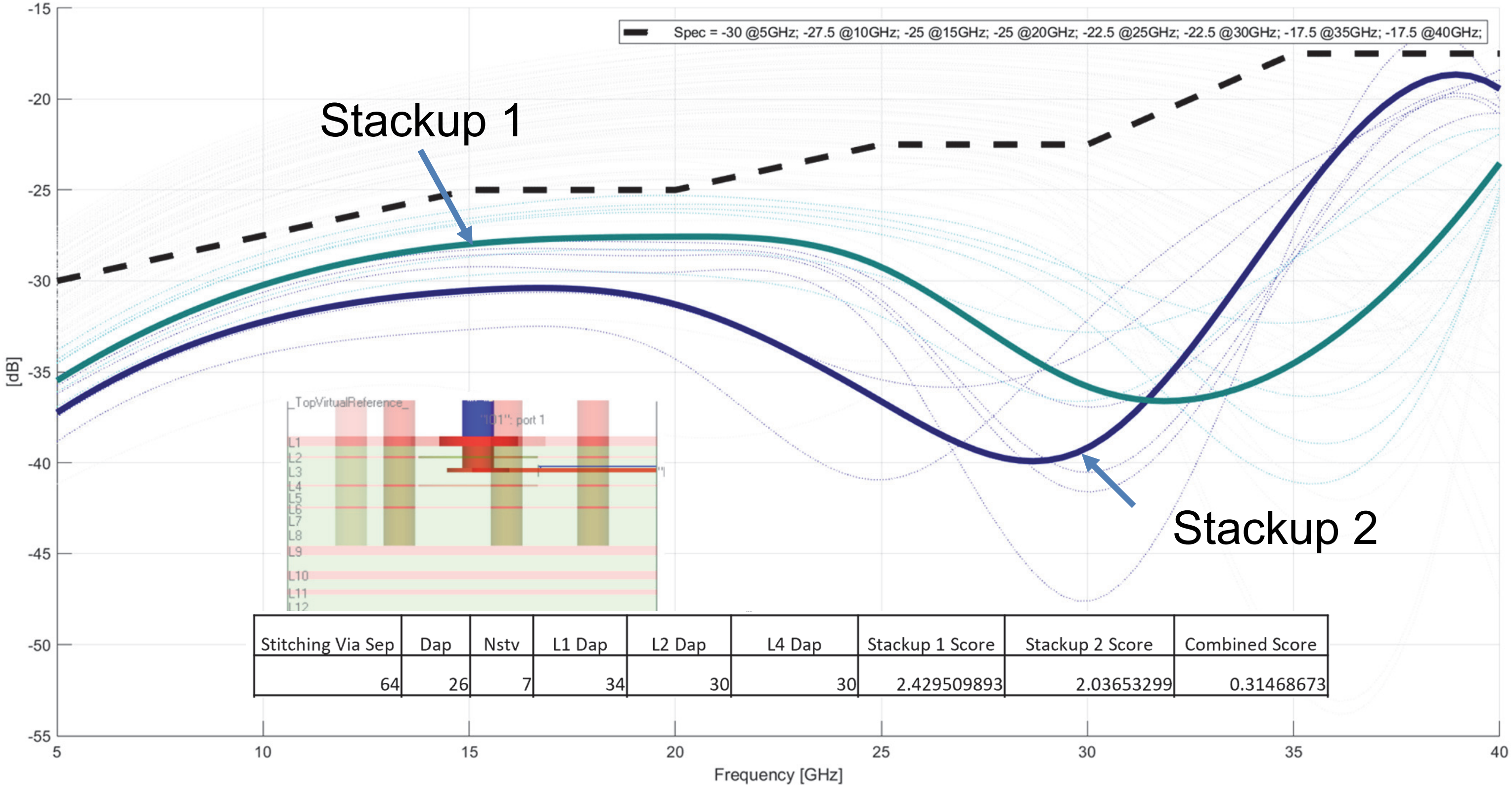


Stitching Via Sep	Dap	Nstv	L1 Dap	L2 Dap	L4 Dap	Stackup 1 Score	Stackup 2 Score	Combined Score
64	26	7	34	30	30	2.429509893	2.03653299	0.31468673
64	26	7	36	32	26	1.64567054	2.717909333	0.309837936
64	26	7	34	30	28	0.746389116	3.987584796	0.307893391
64	26	7	34	30	32	2.656124073	0.718457578	0.241546998

Vendor A

Best Configuration for L3

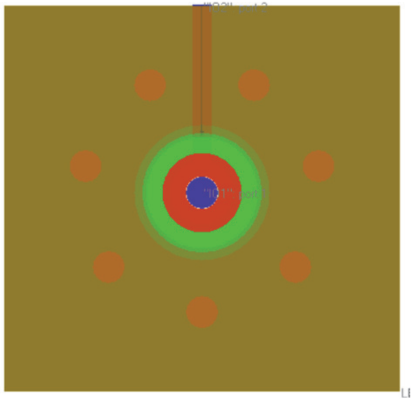
Same layout in 2 similar stackups

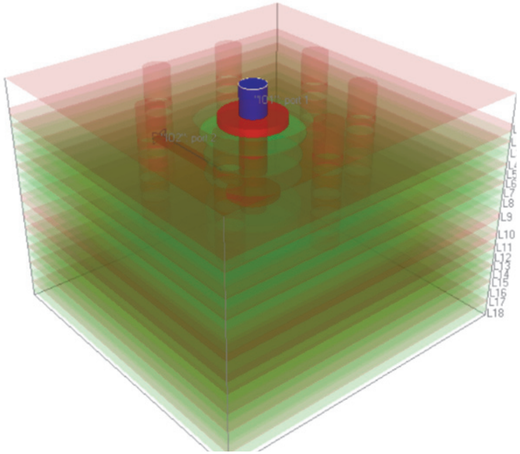


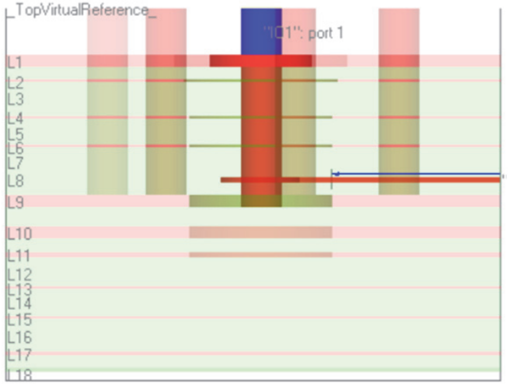
Stitching Via Sep	Dap	Nstv	L1 Dap	L2 Dap	L4 Dap	Stackup 1 Score	Stackup 2 Score	Combined Score
64	26	7	34	30	30	2.429509893	2.03653299	0.31468673

Vendor A

Best Configurations for L8





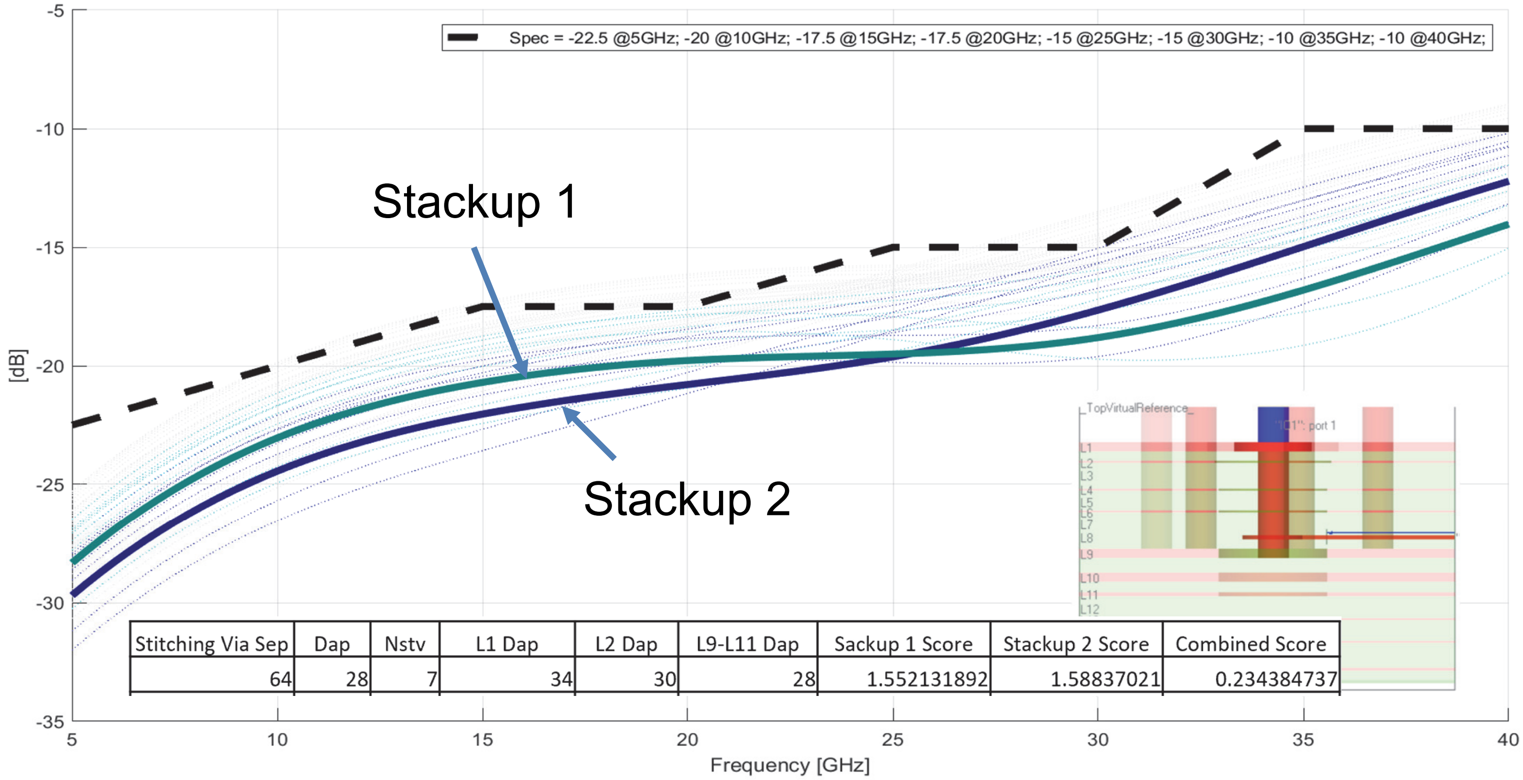


Stitching Via Sep	Dap	Nstv	L1 Dap	L2 Dap	L9-L11 Dap	Sackup 1 Score	Stackup 2 Score	Combined Score
64	28	7	34	30	28	1.552131892	1.58837021	0.234384737
64	30	7	34	30	30	1.510996014	0.574953612	0.192068919
64	28	7	36	32	28	0.814770212	0.85220771	0.176486944
64	26	7	34	30	26	0.231073771	1.413085464	0.157979642

Vendor A

Best Configuration for L8

Same layout in 2 similar stackups

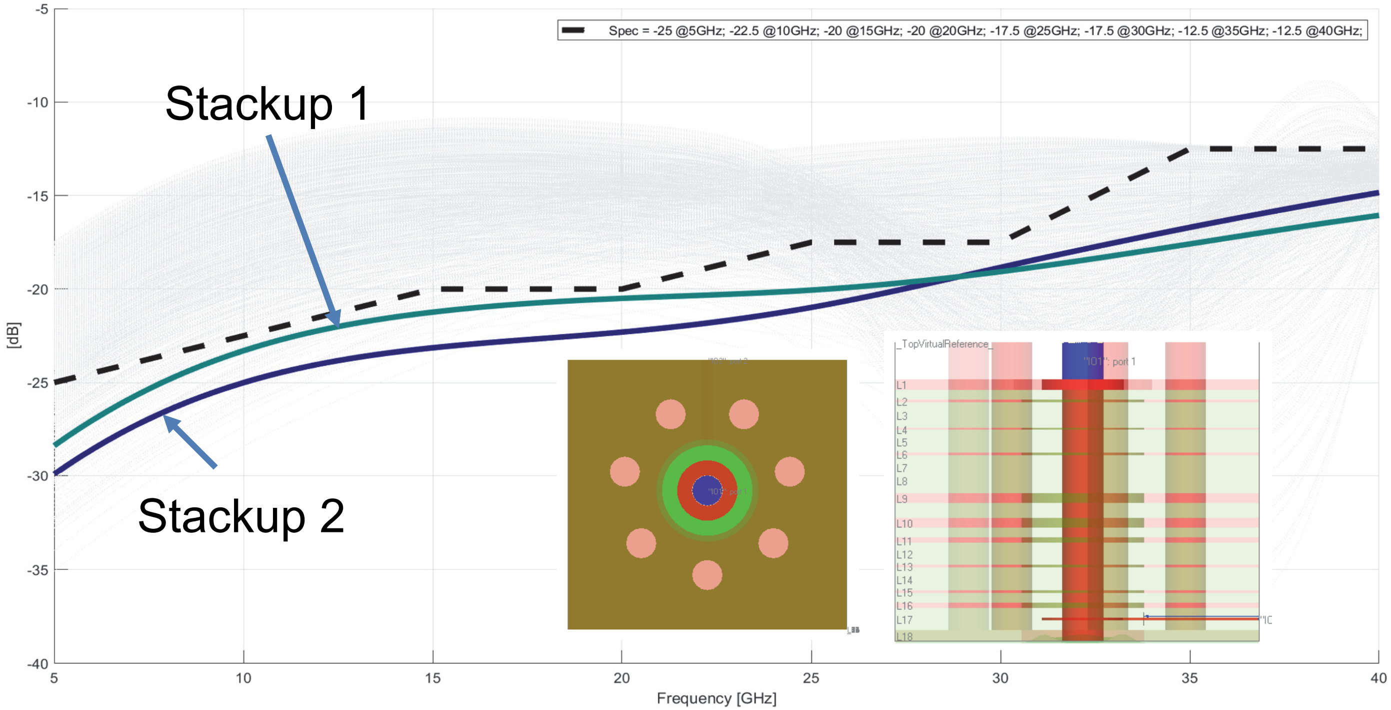


Stitching Via Sep	Dap	Nstv	L1 Dap	L2 Dap	L9-L11 Dap	Sackup 1 Score	Stackup 2 Score	Combined Score
64	28	7	34	30	28	1.552131892	1.58837021	0.234384737

Vendor A

Best Configuration for L17

Can we do better?



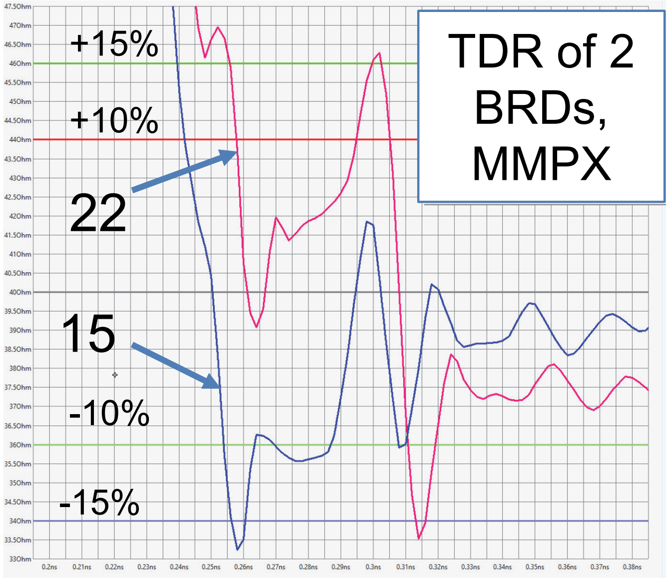
Vendor B

Via Drill	St. Via Drill	Stitching Via Sep	Dap	Nstv	L1 Dap	L18 Dap	Stackup 1 Score	Stackup 2 Score	Combined Score
10	10	56	30	7	34	30	0.73156839	0.142555438	0.112078934

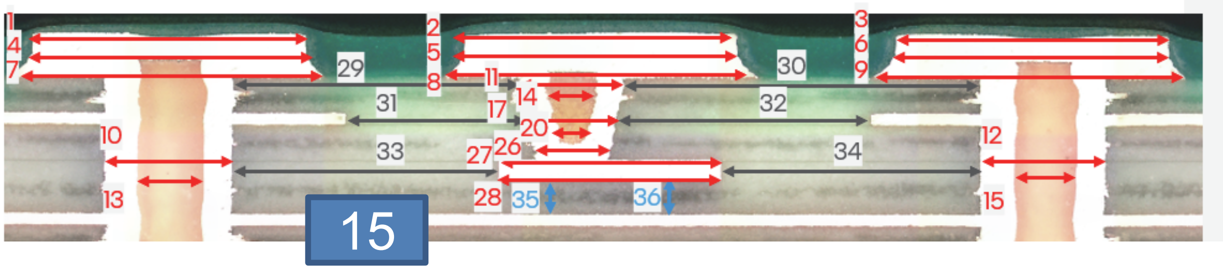
OUTLINE

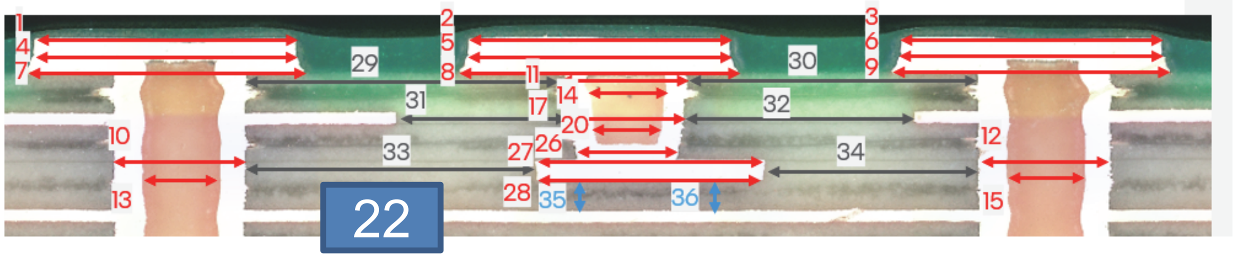
- Introduction
- Bandwidth and Localization
- Design of Vias for Two Stackups
- Reality Check – Cross-Sectioning and TDR
- New Approach to Viahole Design
- Conclusion

Vendor A: L3

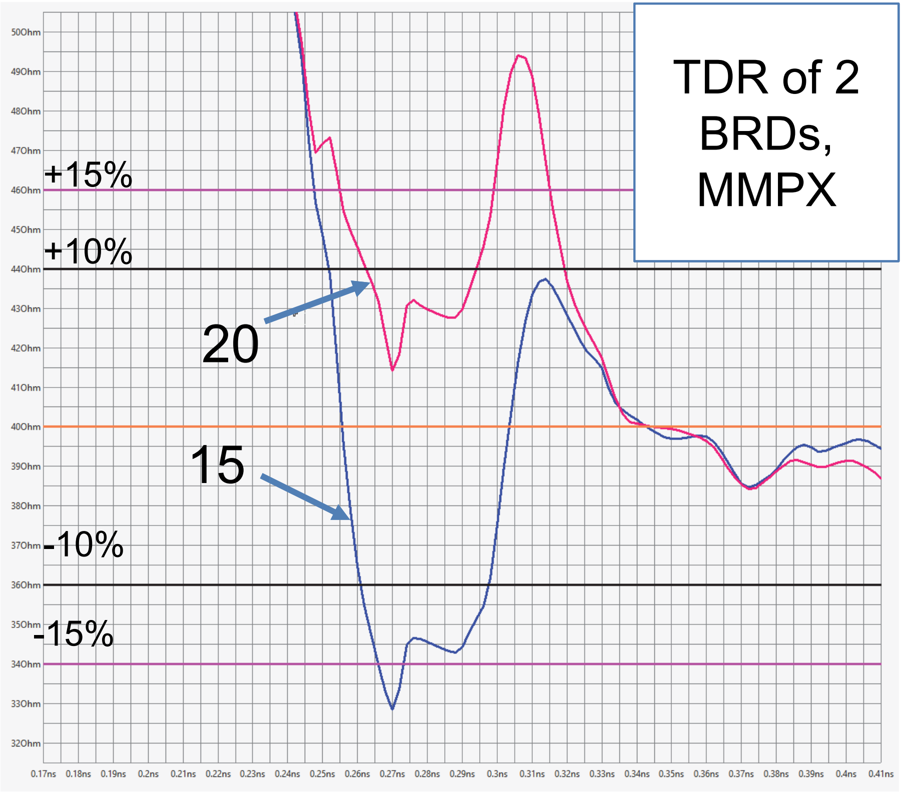


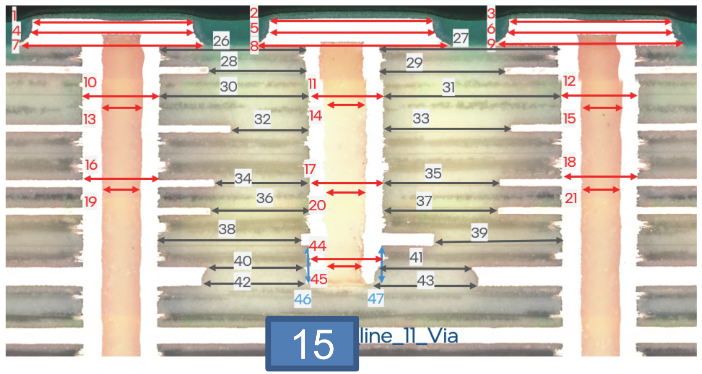
Name	Length [mil]	brd 15		brd22	
29	19.34	-4.66	21.44	1.88	-2.1
30	24		19.56		4.44
31	12.21	-5.05	11.76	-3.73	0.45
32	17.26		15.49		1.77
33	18	0.48	19.65	5.23	-1.65
34	17.52		14.42		3.1

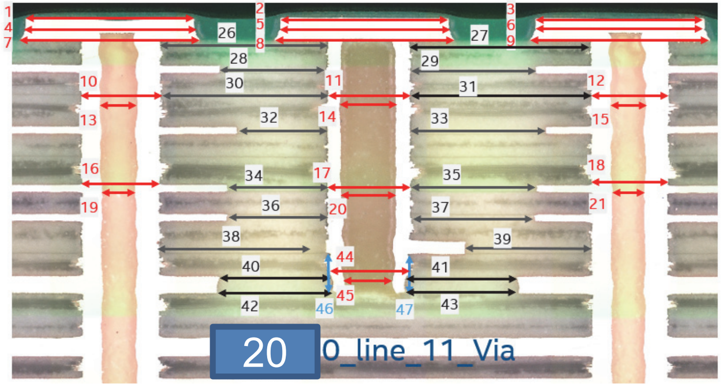




Vendor B: L8

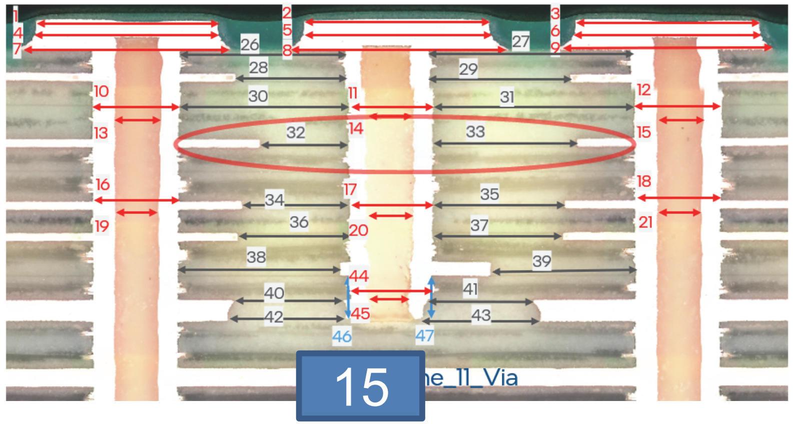

TDR of 2 BRDs, MMPX
+15%
+10%
-10%
-15%
20
15
50Ohm
49Ohm
48Ohm
47Ohm
46Ohm
45Ohm
44Ohm
43Ohm
42Ohm
41Ohm
40Ohm
39Ohm
38Ohm
37Ohm
36Ohm
35Ohm
34Ohm
33Ohm
32Ohm
0.17ns 0.18ns 0.19ns 0.2ns 0.21ns 0.22ns 0.23ns 0.24ns 0.25ns 0.26ns 0.27ns 0.28ns 0.29ns 0.3ns 0.31ns 0.32ns 0.33ns 0.34ns 0.35ns 0.36ns 0.37ns 0.38ns 0.39ns 0.4ns 0.41ns

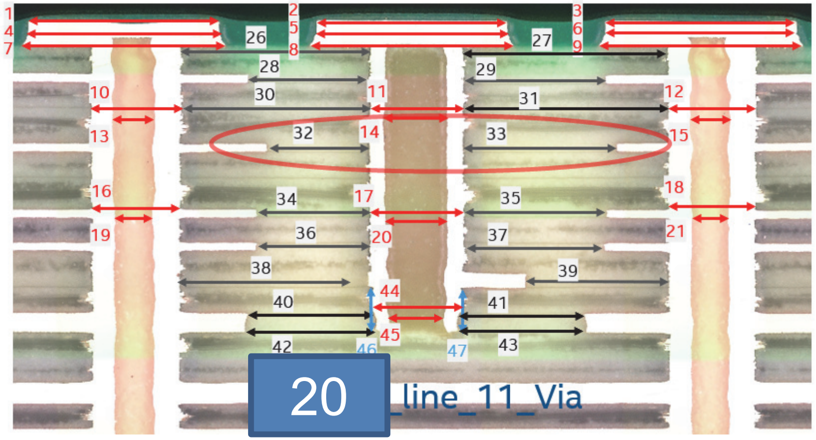

15
line_11_Via


20
0_line_11_Via

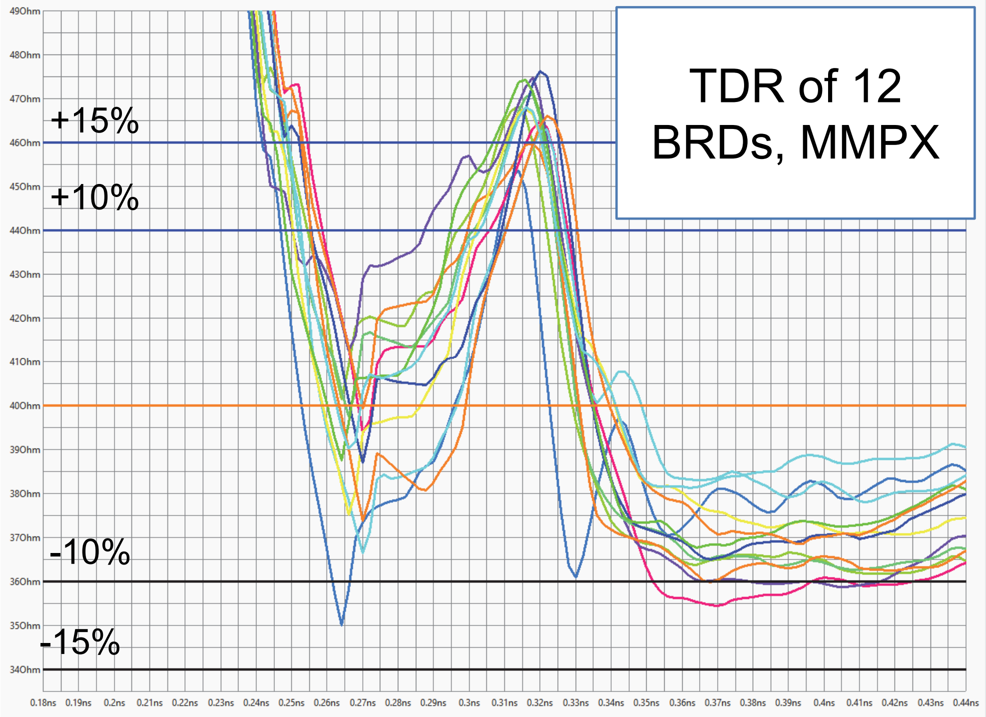
Vendor B: L8

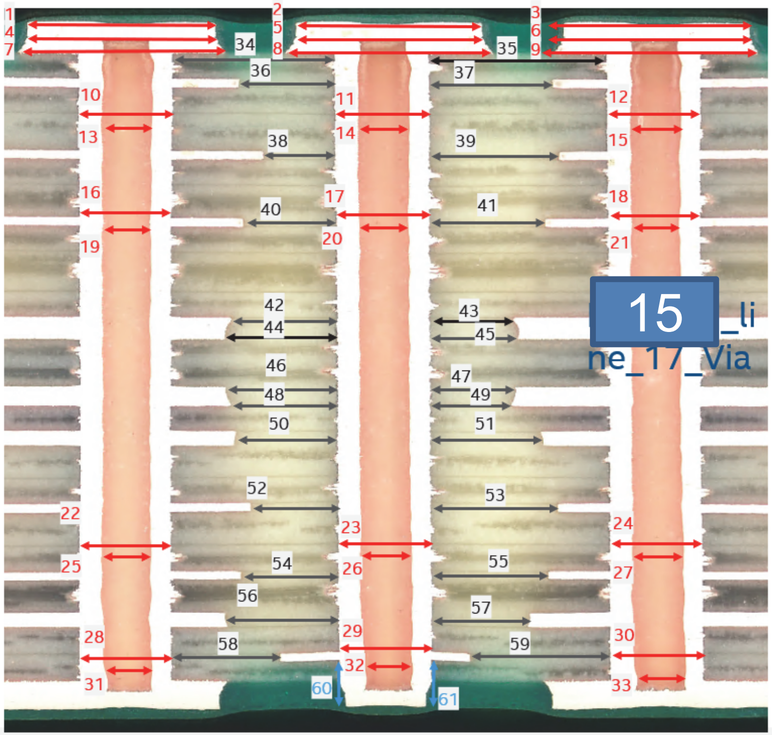
Name	15	Diff.	20	Diff.	pcb2pcn
25	4.45		3.8		0.65
26	16.5	-3.64	17.89	-1.42	-1.39
27	20.14		19.31		0.83
28	11.03	-3.07	11.45	-1.97	-0.42
29	14.1		13.42		0.68
30	16.92	-3.24	17.81	-1.54	-0.89
31	20.16		19.35		0.81
32	8.88	-5.53	9.66	-4.84	-0.78
33	14.41		14.5		-0.09
34	10.77	-2.45	10.78	-2.69	-0.01
35	13.22		13.47		-0.25
36	11.22	-1.93	10.73	-2.48	0.49
37	13.15		13.21		-0.06
38	16.26	1.7	17.81	4.25	-1.55
39	14.56		13.56		1
40	10.99	0.48	11.96	0.15	-0.97
41	10.51		11.81		-1.3
42	11.83	0.12	12.36	0.25	-0.53
43	11.71		12.11		-0.4
44	7.93		8.51		-0.58
45	3.94		5.2		-1.26





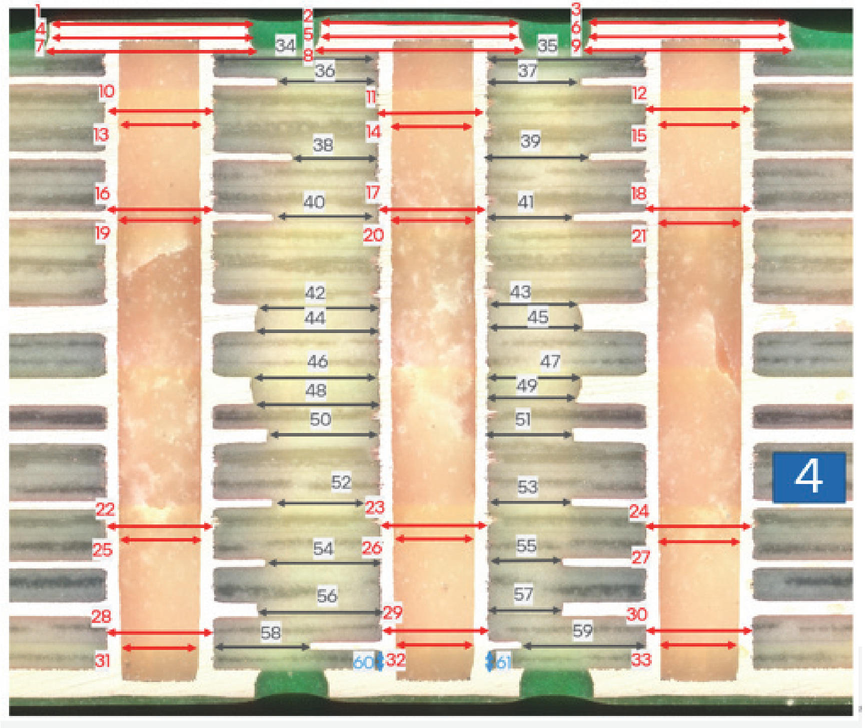
Vendor B: L17

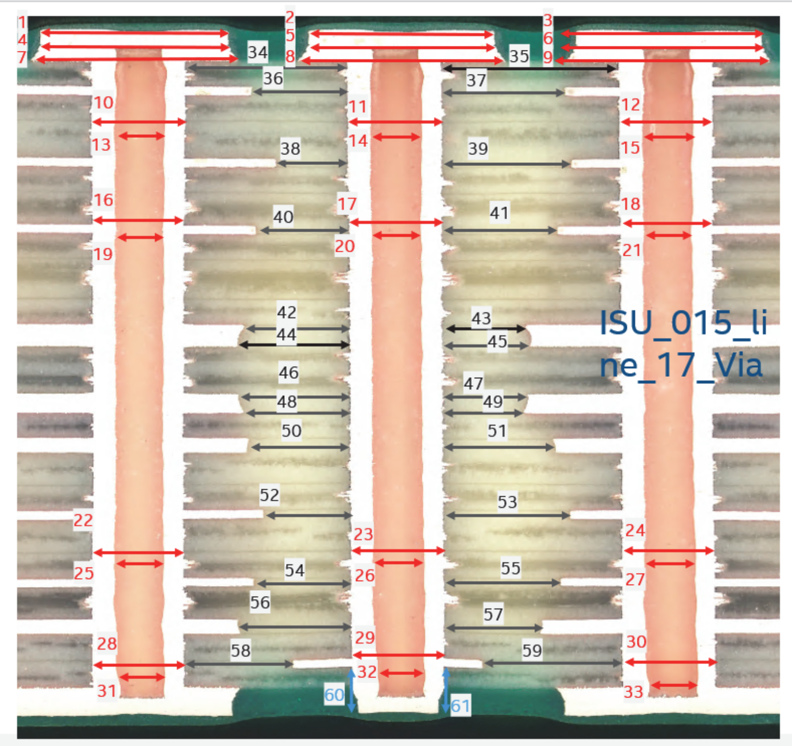

TDR of 12 BRDs, MMPX
+15%
+10%
-10%
-15%
490Ohm
480Ohm
470Ohm
460Ohm
450Ohm
440Ohm
430Ohm
420Ohm
410Ohm
400Ohm
390Ohm
380Ohm
370Ohm
360Ohm
350Ohm
340Ohm
0.18ns 0.19ns 0.2ns 0.21ns 0.22ns 0.23ns 0.24ns 0.25ns 0.26ns 0.27ns 0.28ns 0.29ns 0.3ns 0.31ns 0.32ns 0.33ns 0.34ns 0.35ns 0.36ns 0.37ns 0.38ns 0.39ns 0.4ns 0.41ns 0.42ns 0.43ns 0.44ns


15 _line_17_Via

Possible Explanation of Anisotropy

Misregistration and barrel whiskers increase the capacitance





Summary

vendor	Tline structure		PCB	Status	Issues
A	5	Via_SE_Top_L3_MMPX_40	4	done	L3 pad mis registration – 1.4mil
A	5	Via_SE_Top_L3_MMPX_40	13	done	L3 pad mis registration – -2.45mil
A	7	Via_SE_Top_L5_MMPX_40_BD20_BL6	1	done	Meas L6 void 36-6mil, 37 – 13.5, designed L6 void 28
A	7	Via_SE_Top_L5_MMPX_40_BD20_BL6	2	broken	via misregistered in X and Y direction Meas L4 void 32-18.5mil, 33 – 3, designed L5 void 28
A	11	Via_SE_Top_L8_MMPX_40_landless_L9	2	broken	via misregistered in X and Y direction . Pad shift 6mil. Apad l6 7mil. Pad on L9
A	11	Via_SE_Top_L8_MMPX_40_landless_L9	3	done	Via misregistered 3mil, Apad sizes Pad on L9
B	5	Via_SE_Top_L3_MMPX_40	15	done	Via misregistration 2.3mil
B	5	Via_SE_Top_L3_MMPX_40	22	done	Via misregistration 1mil, pad misregistration 2.6mil
B	7	Via_SE_Top_L5_MMPX_40_BD20_BL6	15	done	Apad L2 1.5mil Via 1.25 Apad L4 2.8mil Pad L5 1.1mil Apad L6 1.3mil
B	7	Via_SE_Top_L5_MMPX_40_BD20_BL6	22	done	Apad L2 1.7mil Via 1.8mil Apad L4 2mil Pad L5 3mil Apad L6 2.3mil
B	11	Via_SE_Top_L8_MMPX_40_landless_L9	15	done	Pad L8 misregistration ~2mil
B	11	Via_SE_Top_L8_MMPX_40_landless_L9	20	done	Pad L8 misregistration ~2mil
B	17	Via_SE_Top_L17_MMPX_40_landless_Bot	15	done	2.6mil misregistration on layer 4
C	17	Via_SE_Top_L17_MMPX_40_landless_Bot	2	done	L4 7mil Apad misregistration
C	17	Via_SE_Top_L17_MMPX_40_landless_Bot	3	done	L2, L4, L16, L17 pad 5-6mil Apad misregistration
C	17	Via_SE_Top_L17_MMPX_40_landless_Bot	4	done	

Can we do better?

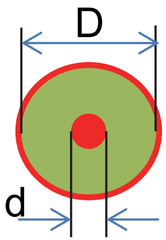
OUTLINE

- Introduction
- Bandwidth and Localization
- Design of Vias for Two Stackups
- Reality Check
- New Approach to Viahole Design
- Conclusion

Revised Viaholes Design Goals and Process

- Goals:
  - Ensure localization – reduce coupling
  - Make it transparent to signal – reduce reflections
  - Use one via design for multiple similar stackups
  - **Reduce sensitivity to manufacturing variations**
  - **Must be simple geometry**
- **Process**
  - Divide via into middle and end sections
  - Design middle section as substrate integrated waveguide with minimal sensitivity to antipads
  - Design end sections as TEM-to-TEM wave transitions as simple as possible

Single Ended Via – Middle Section



Coaxial -> **Substrate Integrated Coaxial Waveguide (SICW)**

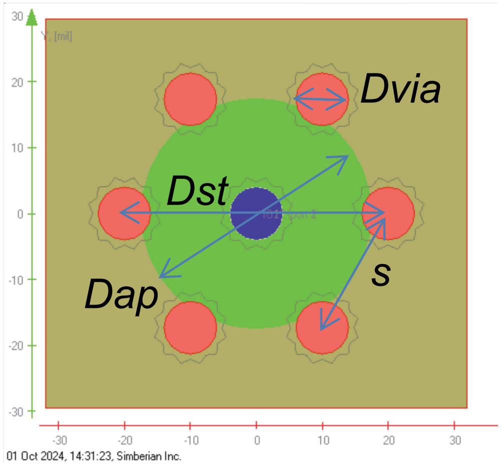
$$D = Dst - \frac{d^2}{0.95 * s}$$

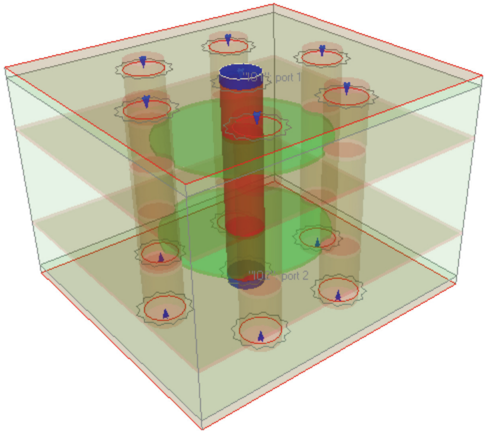
$$d = Dvia$$

$$s < 0.4\lambda \qquad D_{ap} \cong D$$

Single-mode limit is defined by mode TE11:

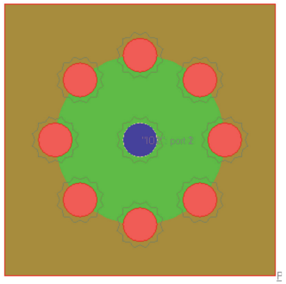
$$f_{cutoff} \approx \frac{2c}{\pi(d + D)\sqrt{\varepsilon}}$$





Dk = 3, Dvia=8mil, Dst=40mil, s=21mil → $f_{cutoff} \approx 96.4\ GHz$ (<AWG30)

Dk = 3, Dvia=4mil, Dst=20mil, s=7.8mil → $f_{cutoff} \approx 199\ GHz$ (<AWG36)

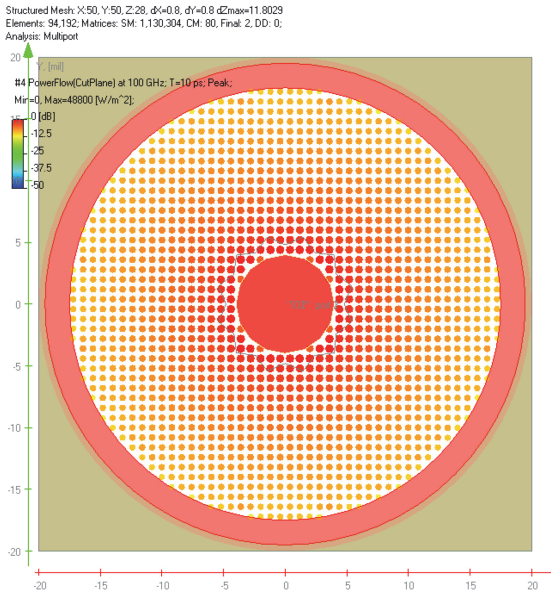


E. R. Pillai, "Coax via technique to reduce crosstalk and enhance impedance match at vias in high-frequency multilayer packages verified by FDTD and MoM modeling," in IEEE Transactions on Microwave Theory and Techniques, vol. 45, no. 10, pp. 1981-1985, Oct. 1997.

Bozzi, M.; Georgiadis, A.; Wu, K. "Review of substrate-integrated waveguide circuits and antennas". IET Microwaves, Antennas & Propagation, 2011 ***5*** *(8): 909.*

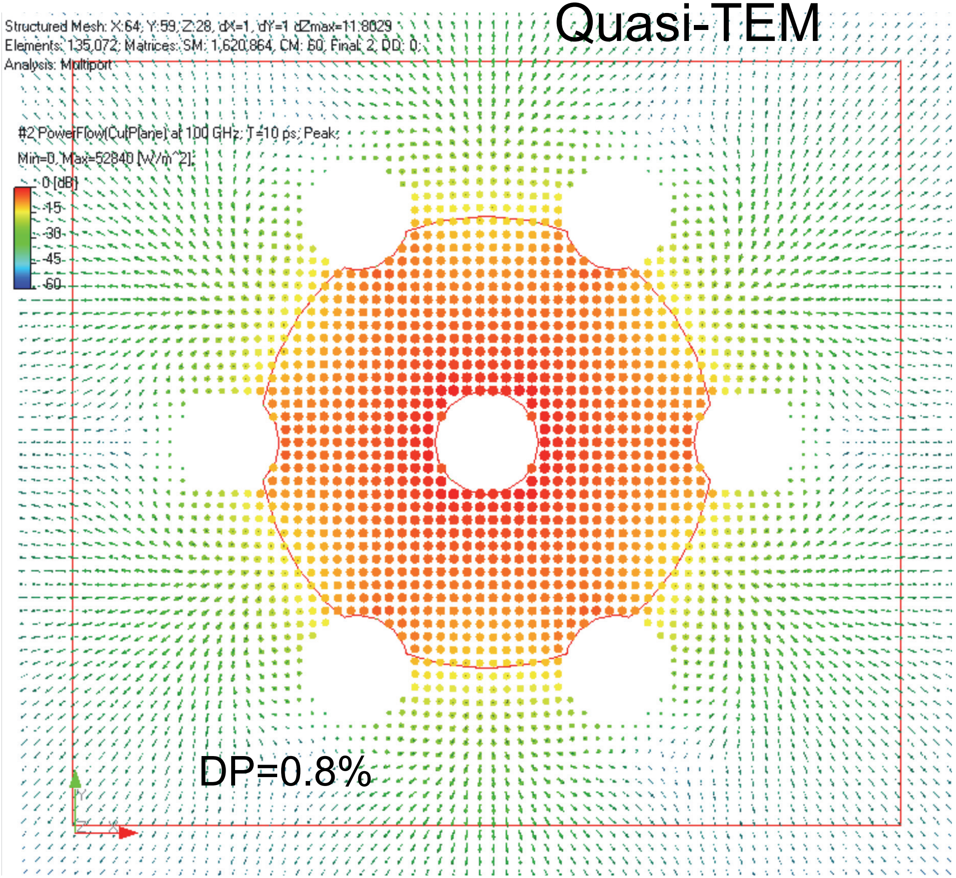
Power Flow Density in SICW at 100 GHz

TEM



DP=0.69%

Quasi-TEM



DP=0.8%

Sensitivity of SICW

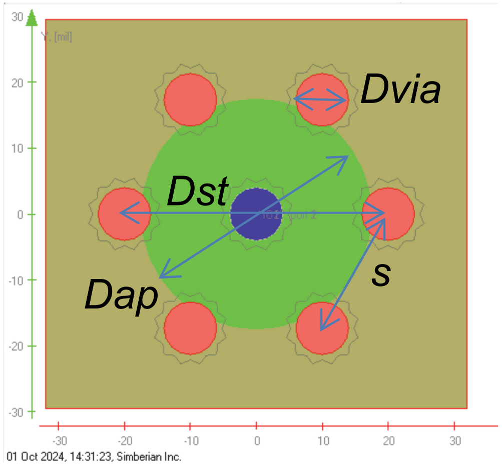
Should be similar to coaxial

$$Z_o \approx \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * ln\left(\frac{D}{d}\right)$$

$$D = d \cdot e^{2\pi Z_o\sqrt{\frac{\varepsilon}{\mu}}}$$

$$Dst = D + \frac{d^2}{0.95 * s}$$

$$D_{ap} \approx D \qquad Dvia = d$$



$$\Delta Z_o \approx -\frac{\Delta\varepsilon}{2\varepsilon} * Z_o$$

10% change in Dk -> only 5% change in Zo (or about -32dB in RL)

$$\Delta Z_o \approx \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * \frac{\Delta D}{D}$$

1mil change in D=40mil -> only 1 Ohm change in Zo (or about -40dB in RL)

$$\Delta Z_o \approx -\frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * \frac{\Delta d}{d}$$

1mil change in d=8mil -> 4.3 Ohm change in Zo (or about -27.7dB in RL)

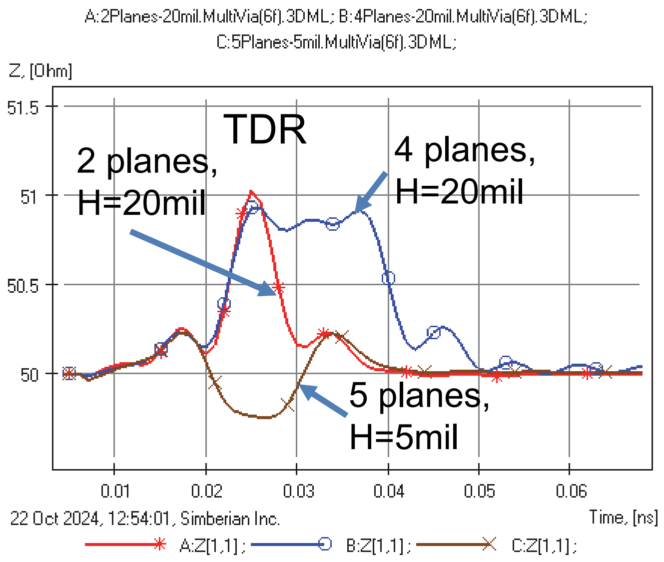
J. B. Preibisch, P. Triverio and C. Schuster, "Sensitivity analysis of via impedance using polynomial chaos expansion," 2015 IEEE 19th Workshop on Signal and Power Integrity (SPI), Berlin, Germany, 2015, pp. 1-4.

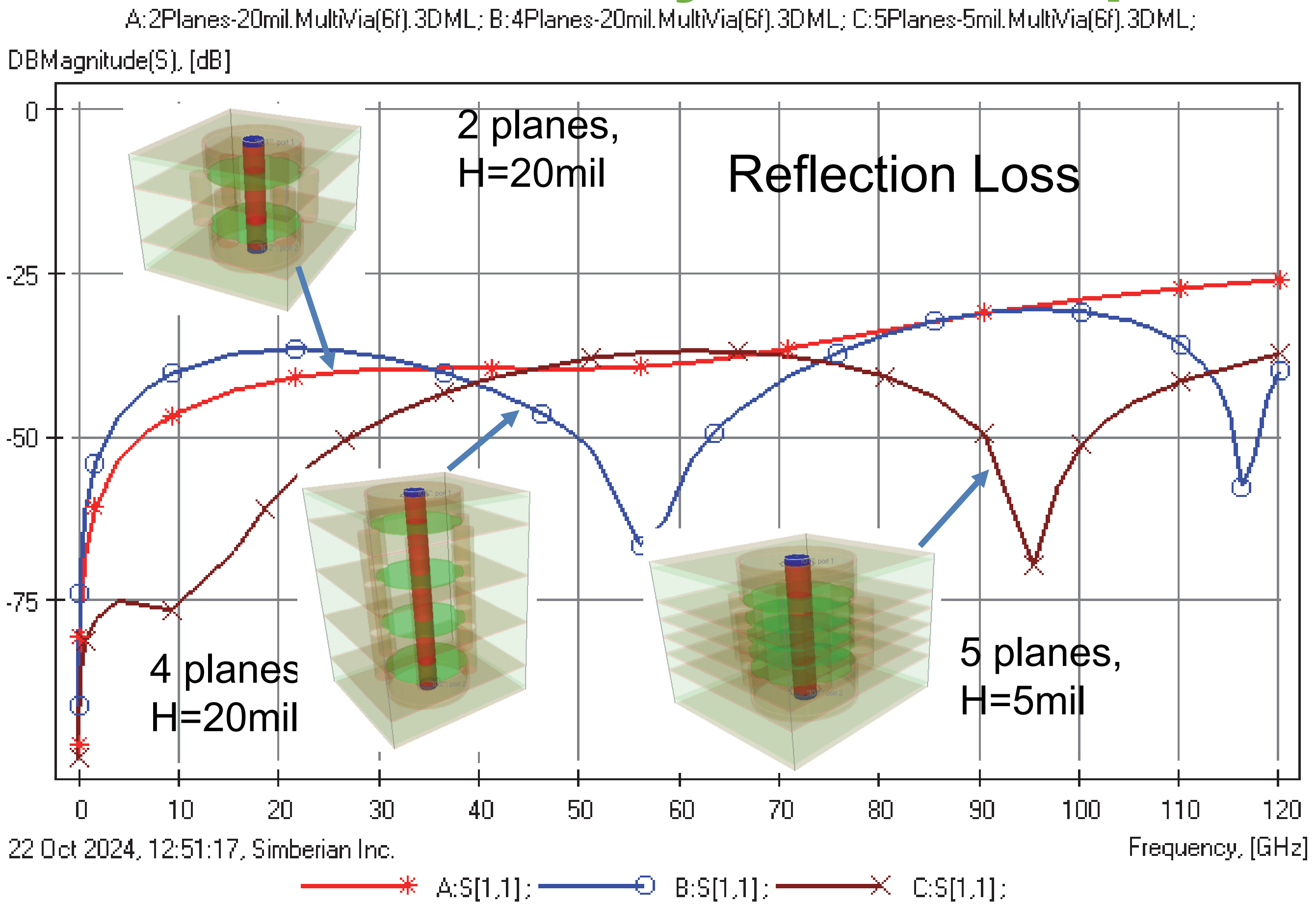
A. Vardapetyan and C. -J. Ong, "Via Design Optimization for High-Speed Differential Interconnects on Circuit Boards," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2020, pp. 1-3.

Middle Section as SICW – Immunity to Stackup

SICW is immune to stackup structure changes

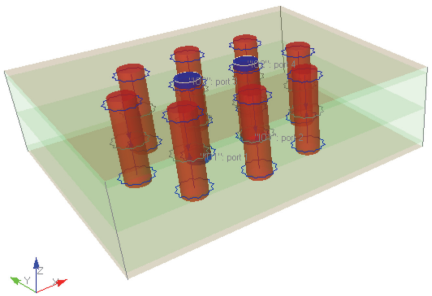
Nstv=6, Dvia=8mil, Dst=40mil, Dap=35mil, Dk=3, LT=0.001

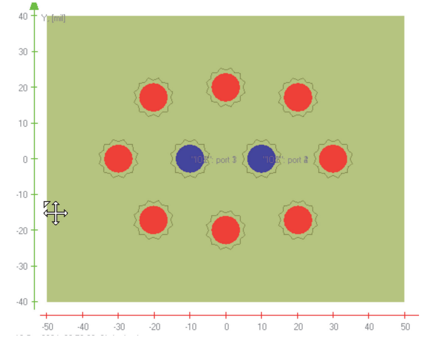


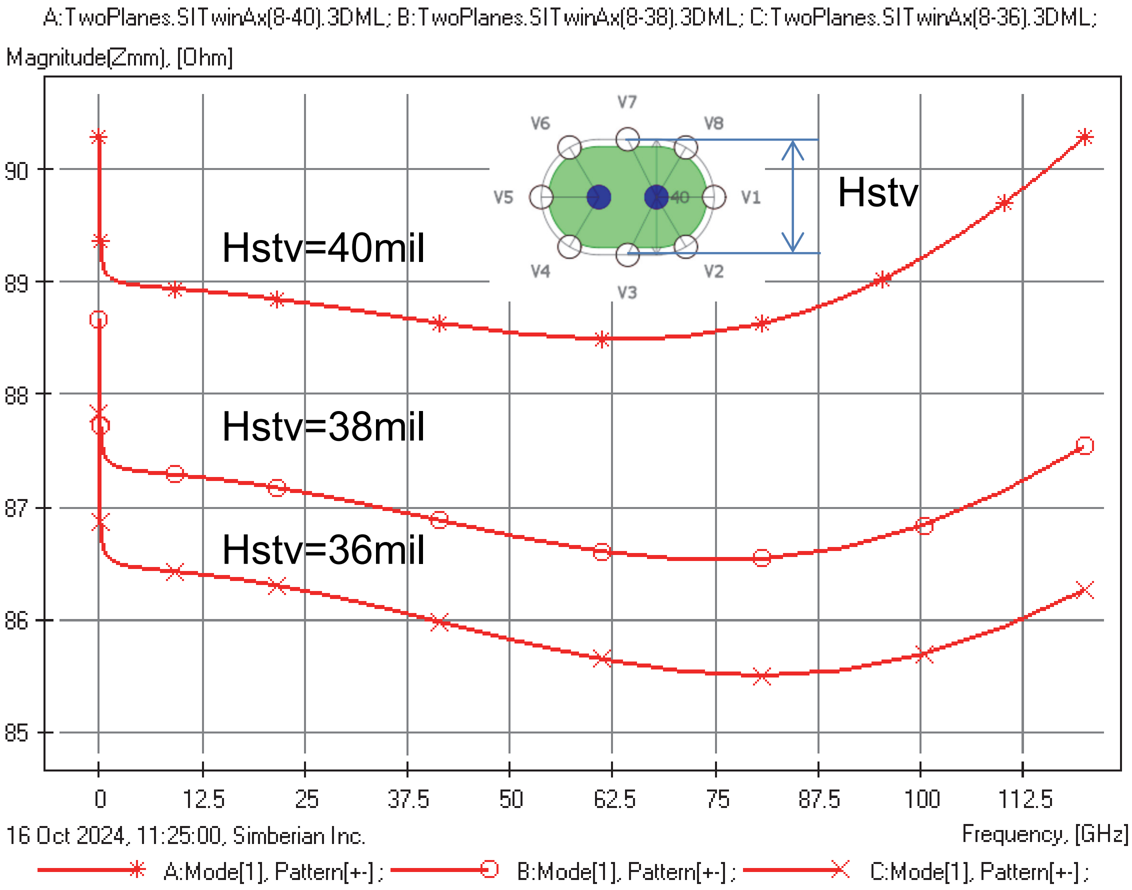


Substrate Integrated TwinAx Waveguide (SITW)

Oval pattern, Nstv=8
H=20mil, Dvv=20mil
Dk=3, LT=0.01

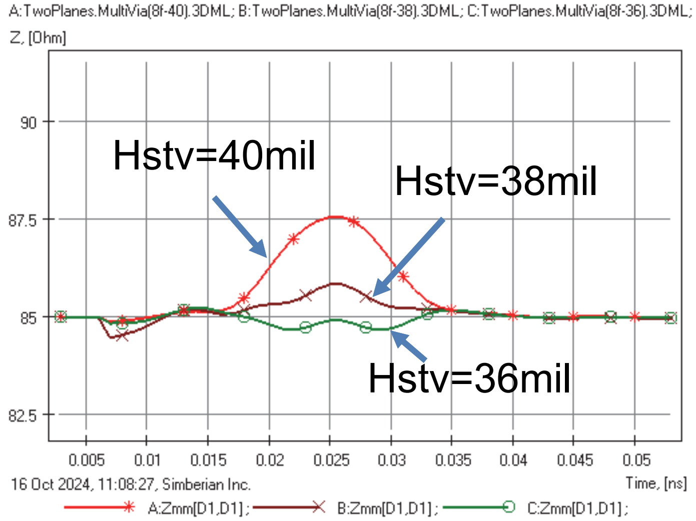


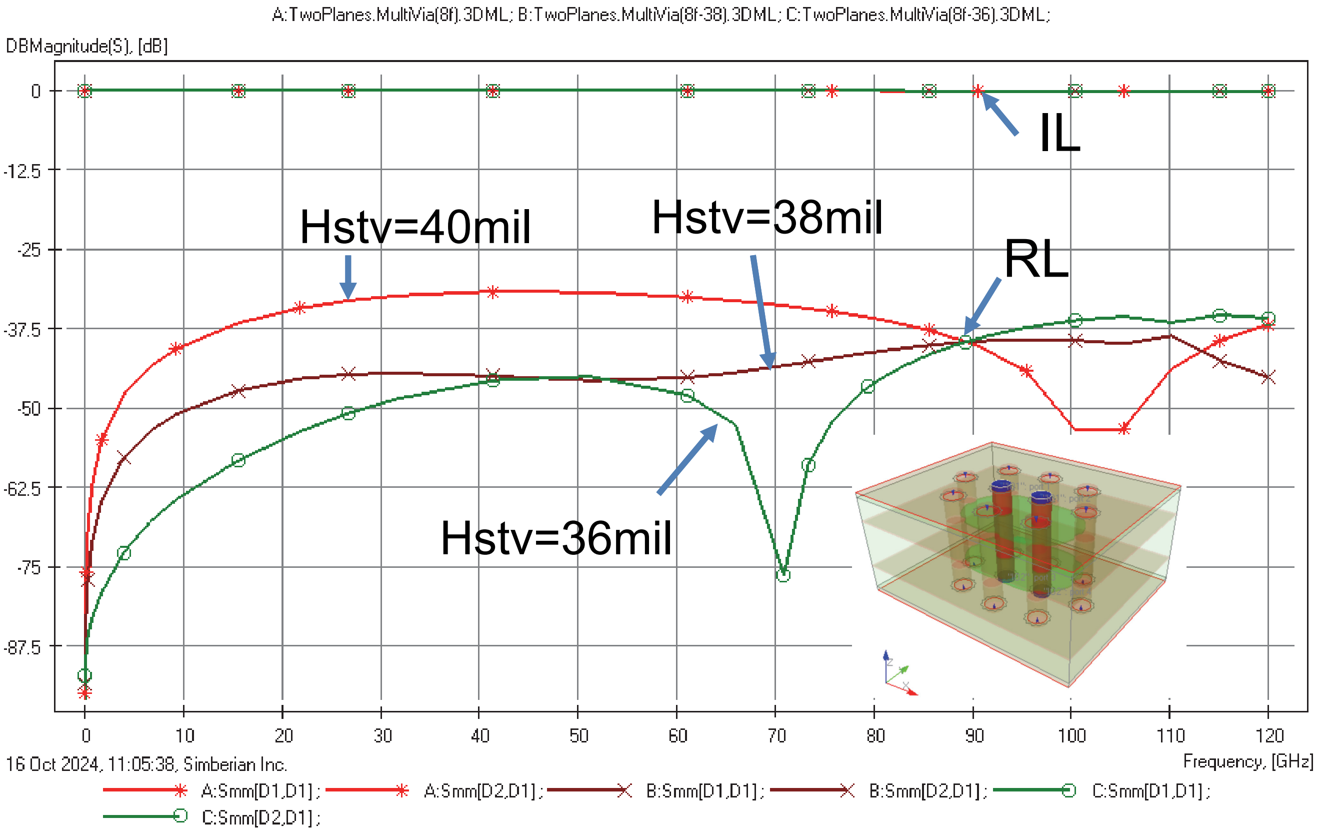




Example of Middle Section as SITW

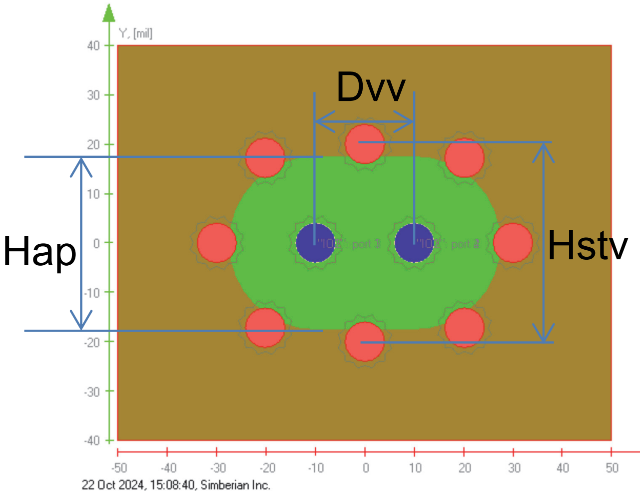
Nstv=8, Dvia=8mil,
Hap=35mil, Dvv=20mil
Dk=3, LT=0.001
Simbeor 3DML, ABC



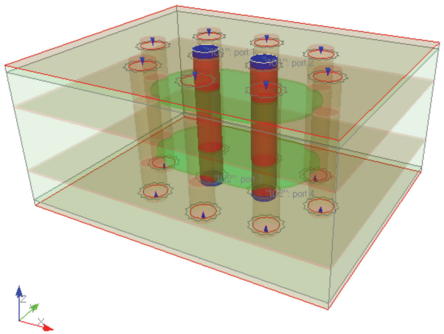


Same SITW in Different Stackups

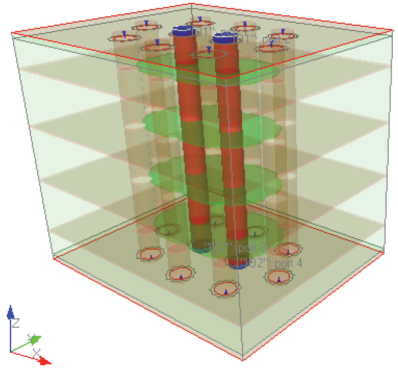
Same XY-plane geometry: Dvia=8mil, Dvv=20mil, Hstv=40mil, Hap=35mil, Dk=3, LT=0.001



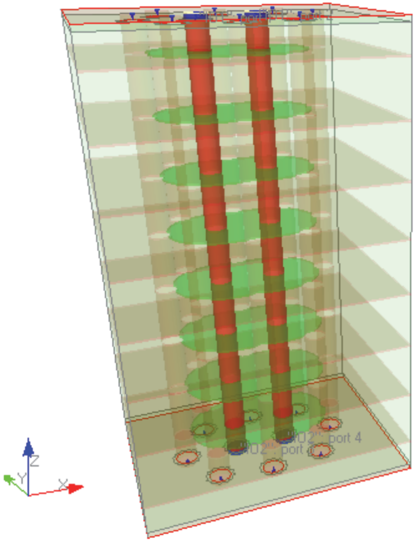
2 Planes, H=20mil



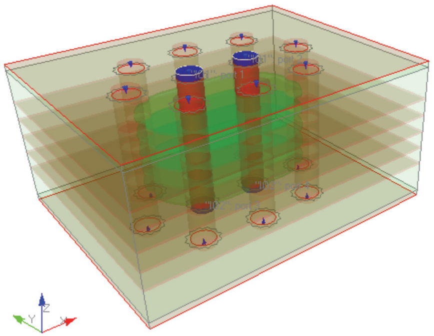
4 Planes, H=20mil



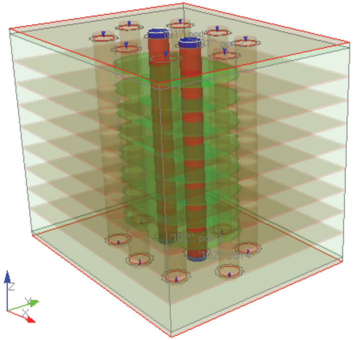
8 Planes, H=20mil



5 Planes, H=5mil

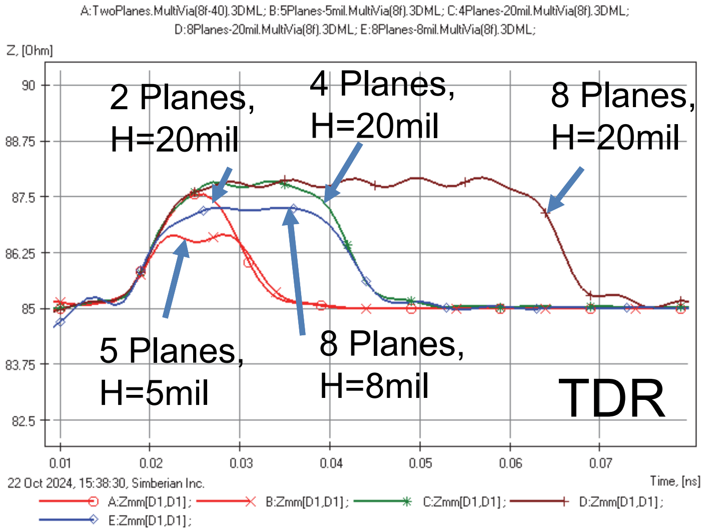


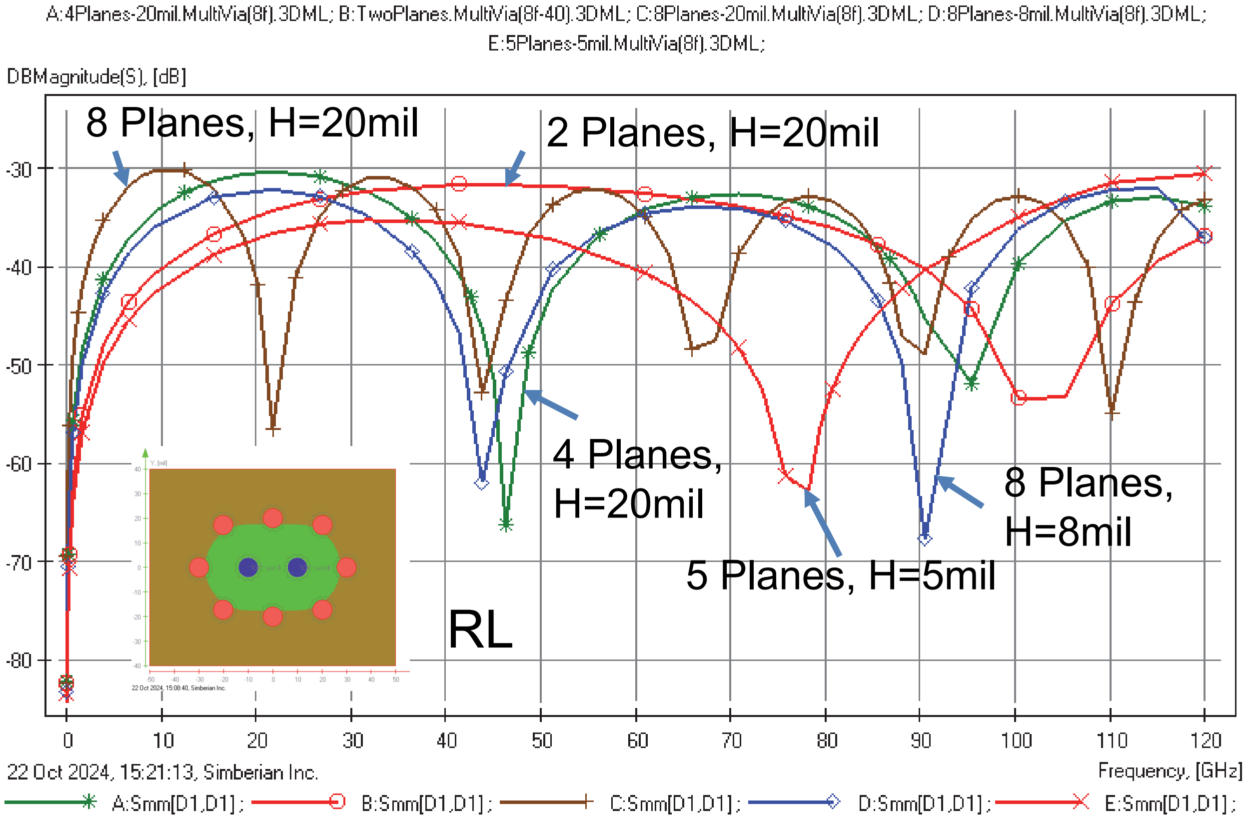
8 Planes, H=8mil



SITW Immunity to Stackup Structure

Same XY-plane geometry: Dvia=8mil, Dvv=20mil, Hstv=40mil, Hap=35mil, Dk=3, LT=0.001
Simbeor 3DML, ABC

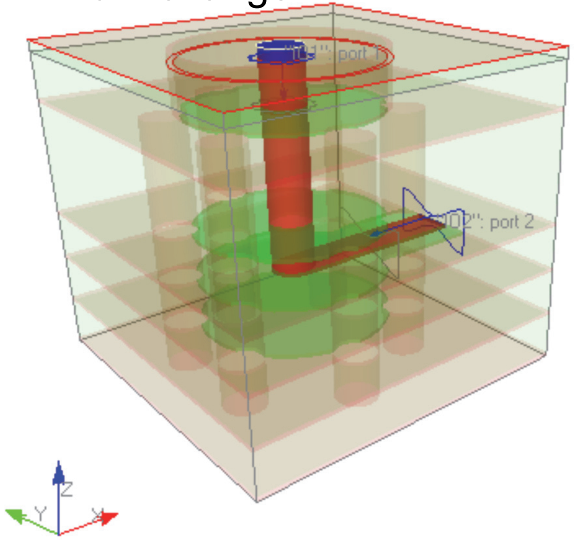




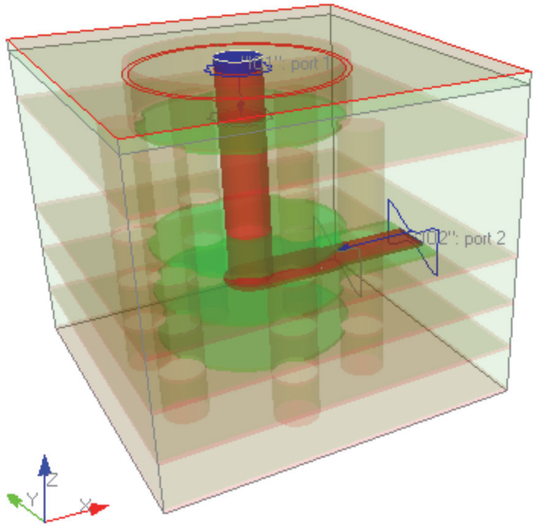
SE Via Vertical to Horizontal Transition (VHT)

Nstv=6, Dvia=8mil, Dst=40mil, Dap=35mil, Dk=3, LT=0.001

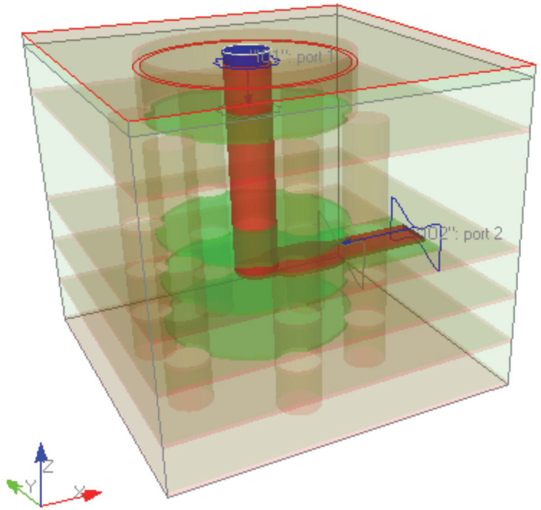
1. No pad, no trace width change



2. Pad + wide trace

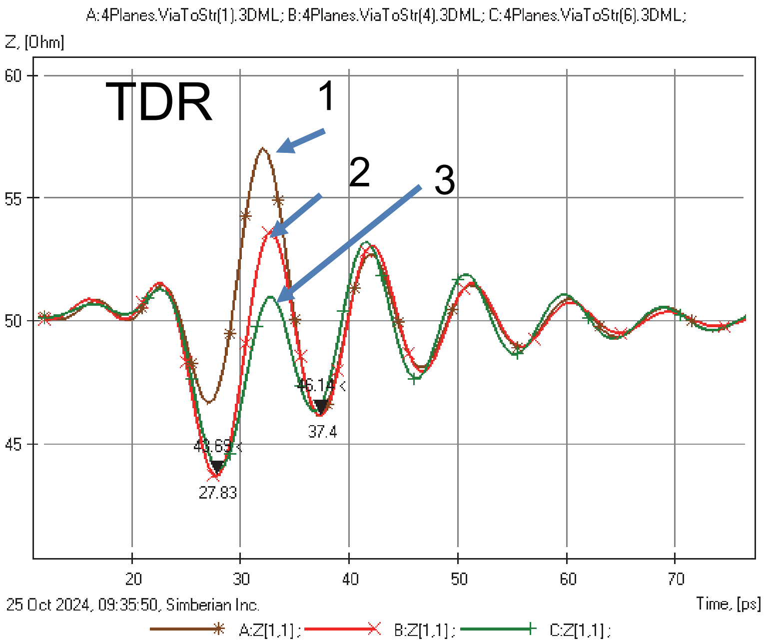


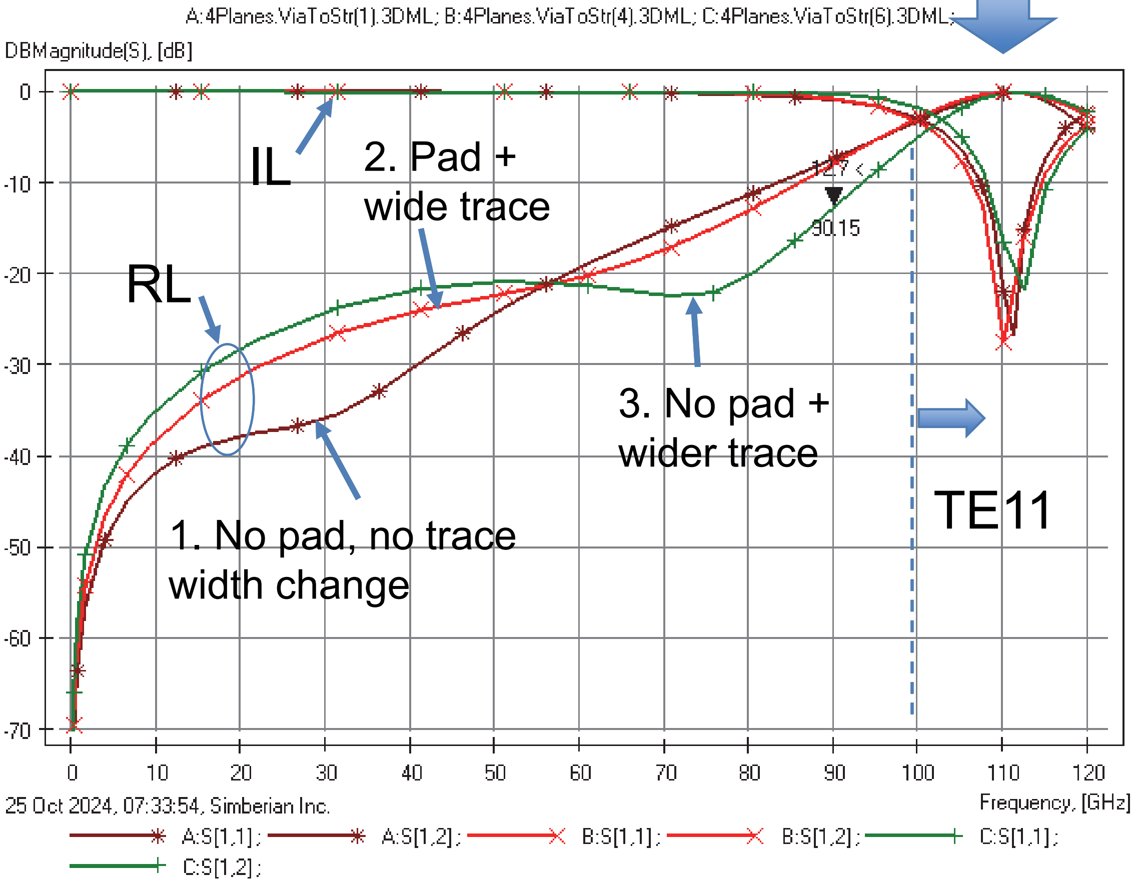
3. No pad + wider trace



SE Via VHT: TDR & S-parameters

Nstv=6, Dvia=8mil, Dst=40mil,
Dap=35mil, Dk=3, LT=0.001

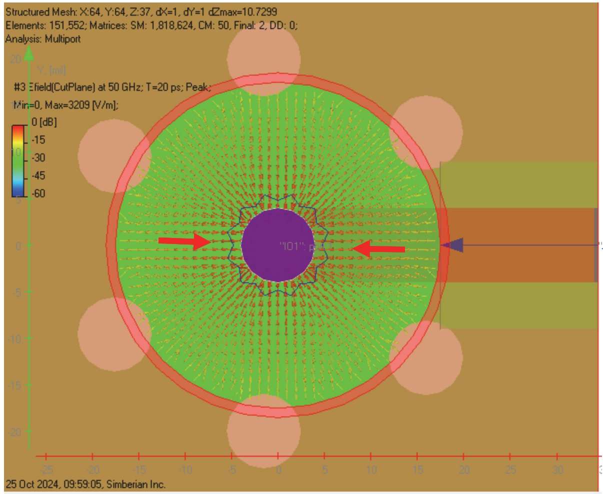




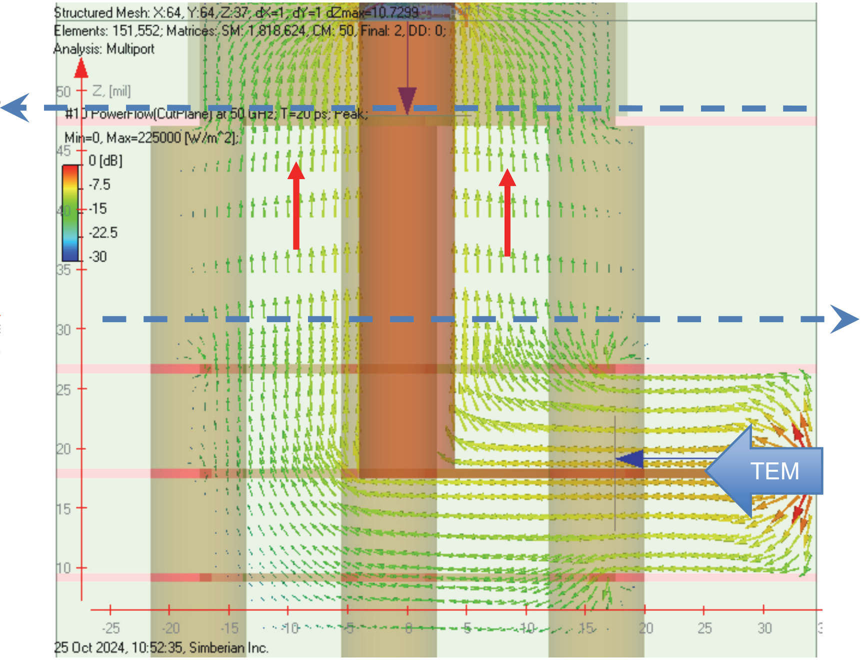
SICW to strip line matching the impedance is not sufficient above 90 GHz!

Mode Transition at VHT: TEM to TEM

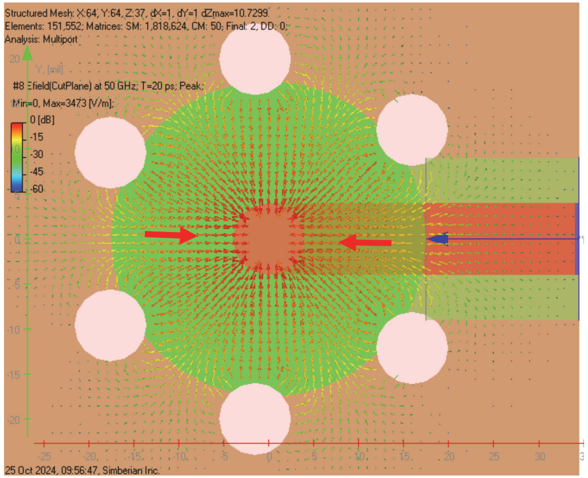
E-fields at 50 GHz - Coax. TEM



Peak PFD at 50 GHz

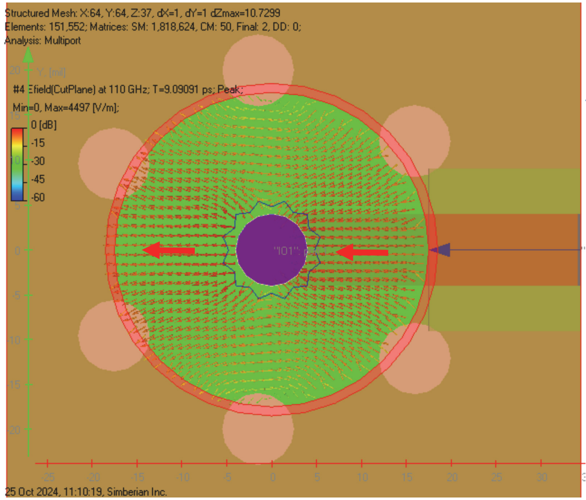


E-field at 50 GHz - SICW Quasi-TEM

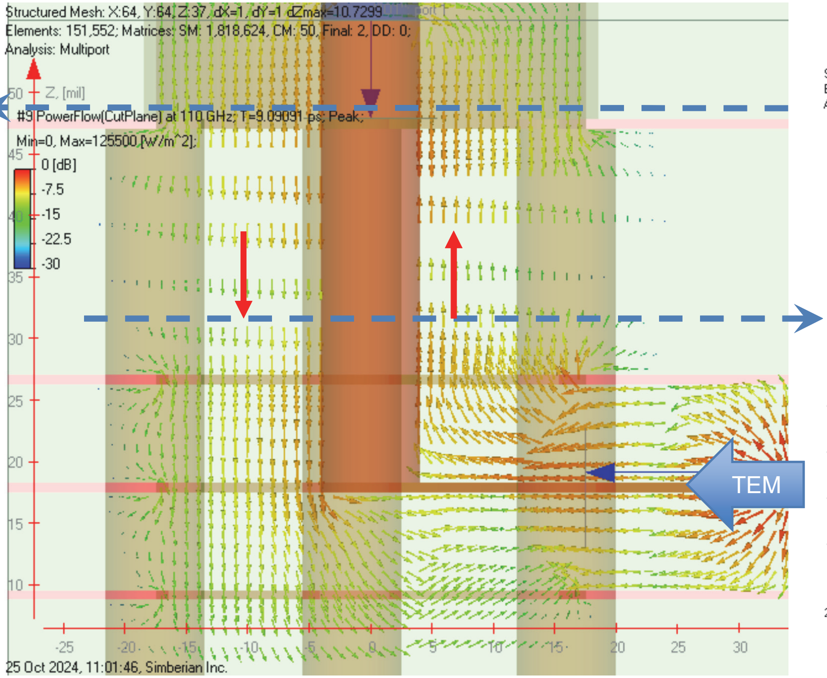


Mode Conversion at VHT: TEM to TE11

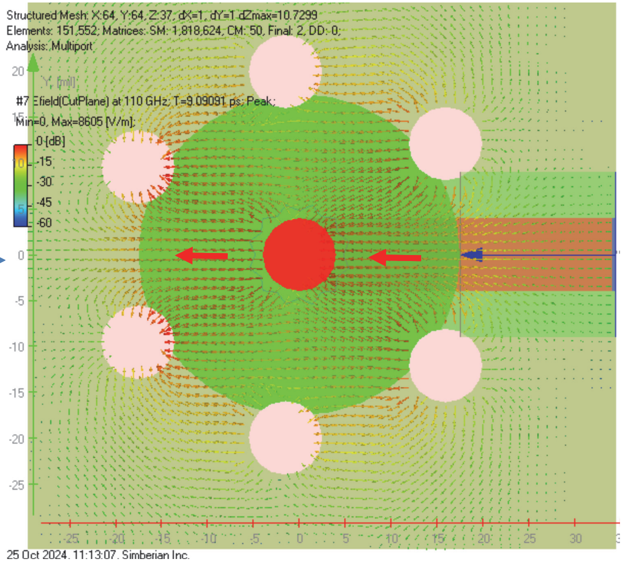
E-field at 110 GHz – Coax. TE11



Peak PFD at 110 GHz

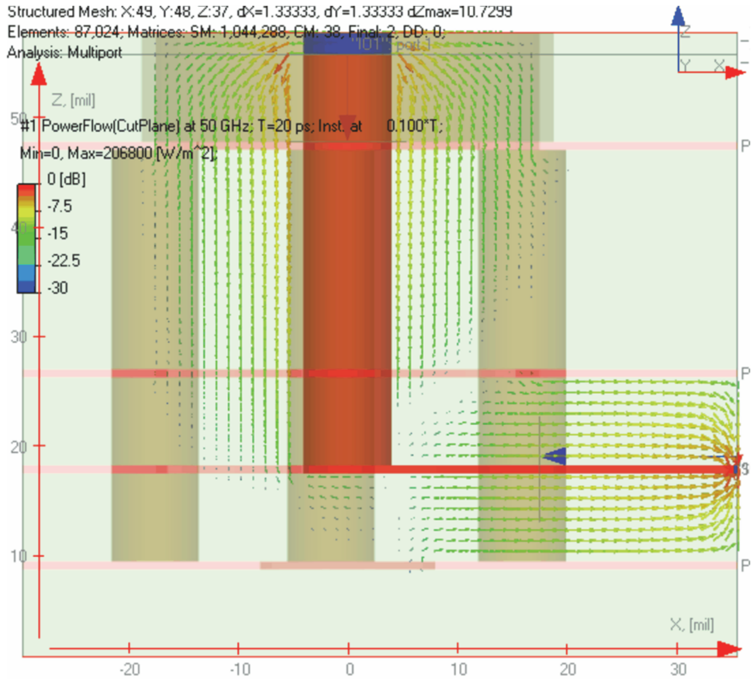


E-field at 110 GHz - SICW Quasi-TE11

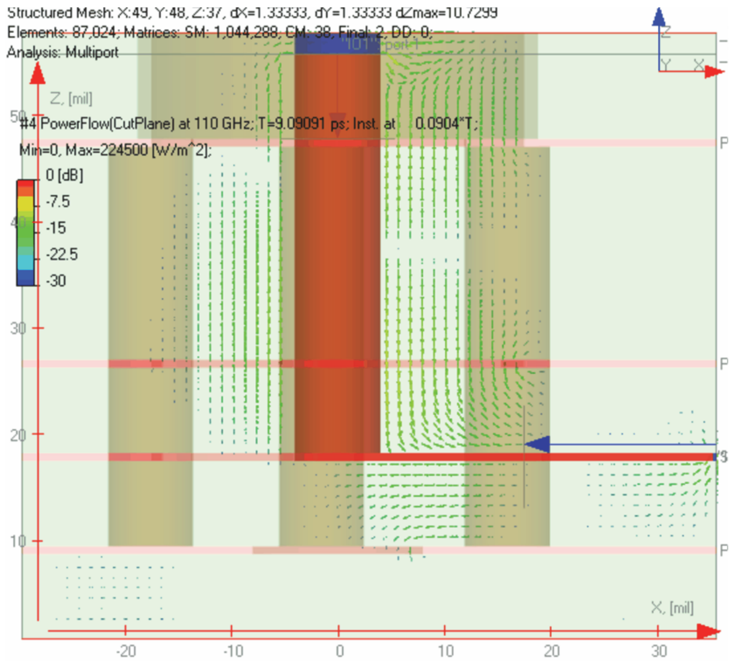


Mode Conversion at VHT (animated)

Peak PFD at 50 GHz: TEM -> TEM

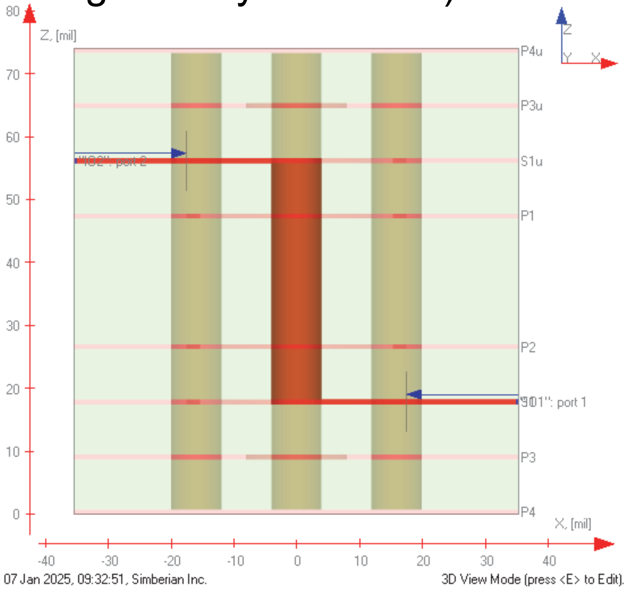


Peak PFD at 110 GHz: TEM ->TE11

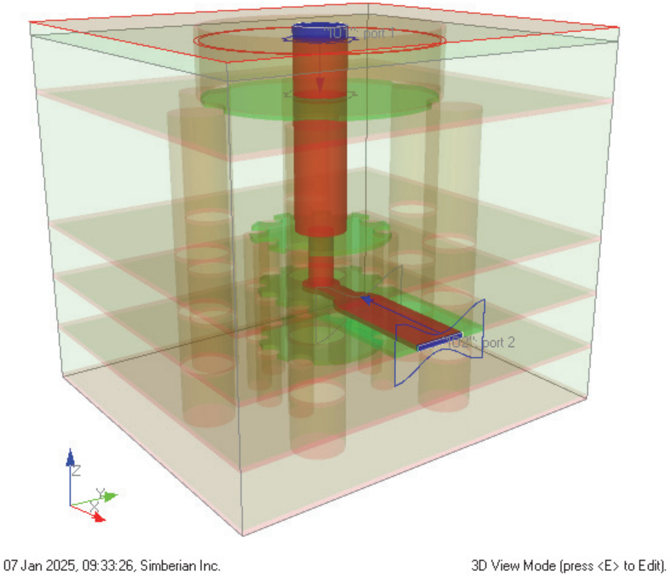


SE Via VHT: How to Reduce Mode Conversion?

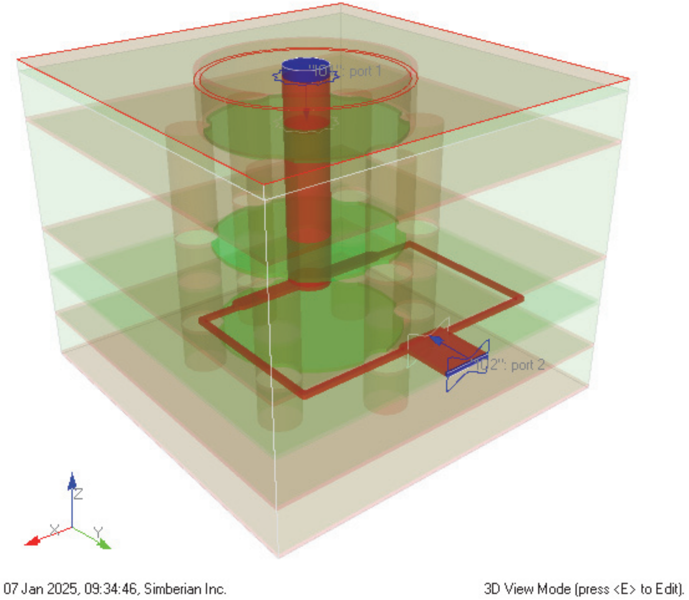
Convert it back (very sensitive to geometry variations)



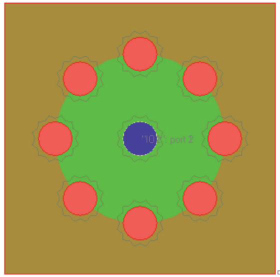
Taper the via (use microvias at the transition)



2-side breakout (narrow strips)

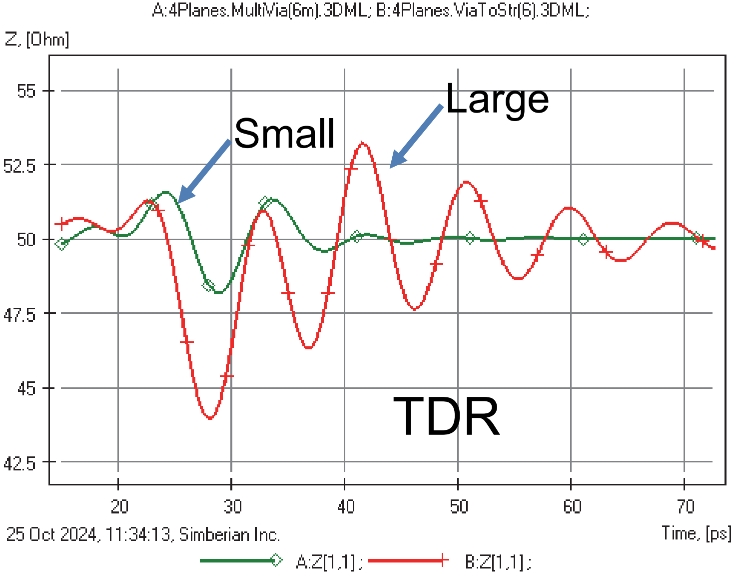


SE Via VHT: How to Extend Bandwidth?

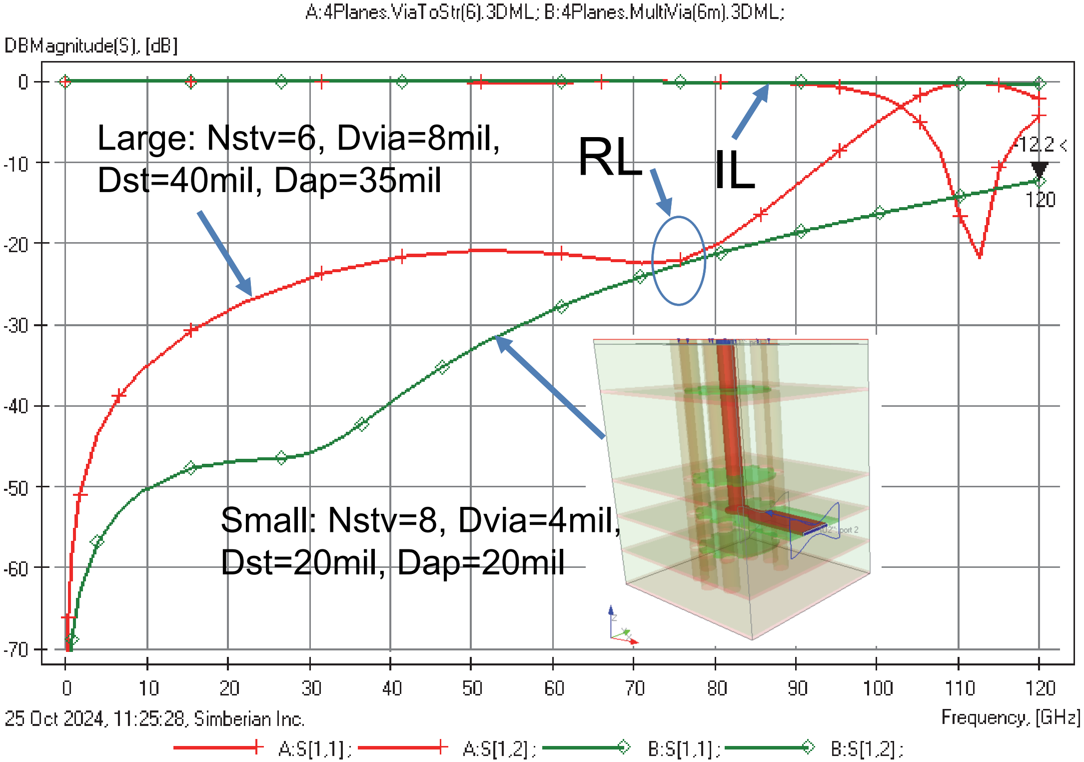


SICW with Nstv=8, Dvia=4mil,
Dst=20mil,
Dk = 3, LT=0.001

$$f_{cutoff} \approx 199\ GHz$$

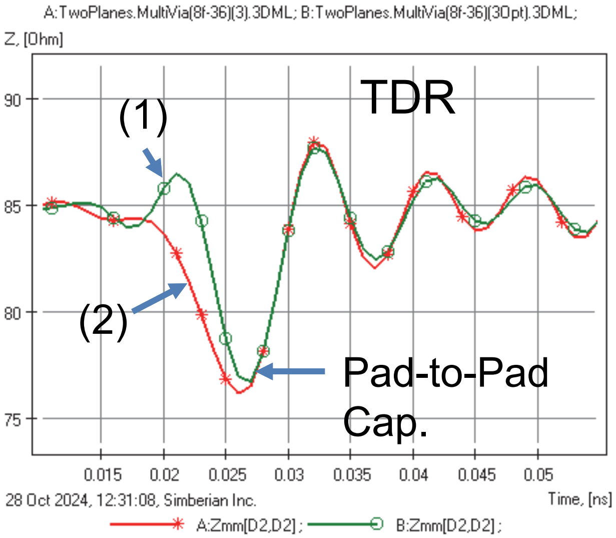


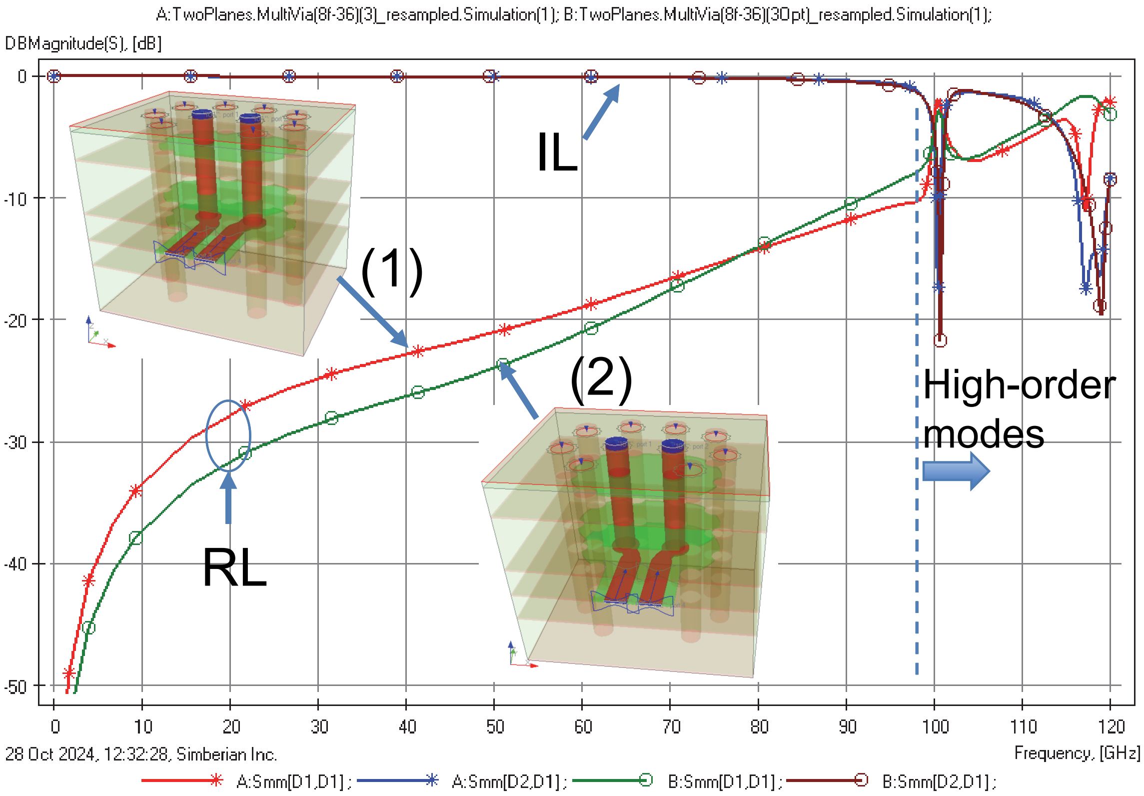
Smaller is better!



Example of Differential VHT

Nstv=8, Dvia=8mil,
Hap=35mil, Hstv=36, Dvv=20mil
Dk=3, LT=0.001
Simbeor 3DML, PEC





Conclusion

- We explored theoretical approaches for designing PCB vias for 112 Gbps and path toward 224-448 Gbps applications
- Formal metrics and critical conditions for via localization up to 120 GHz are discussed
- Direct optimization approach for two stackups showed excessive sensitivity to manufacturing variations
- Waveguiding approach for via design with segmentation into middle and end sections is proposed as an alternative
- Middle sections designed as substrate integrated coaxial or twin ax waveguides are relatively independent of the stackup structure and not sensitive to geometry variations
- New approaches to vertical to horizontal transitions are also proposed
- The waveguiding approach is a work in progress and will undergo further testing in practical scenarios for 448 Gbps applications

Thank you!

QUESTIONS?

Yuriy Shlepnev

Simberian Inc.

Shlepnev@simberian.com | www.simberian.com

Balance of Power: Coupling and Dissipation

$$\boldsymbol{P_{out} = P_{in} - P_{reflected} - P_{dissipated} - P_{leaked} + P_{coupled}}$$

$P_{in} = |a_1|^2\ [Wt], a_2 = 0$

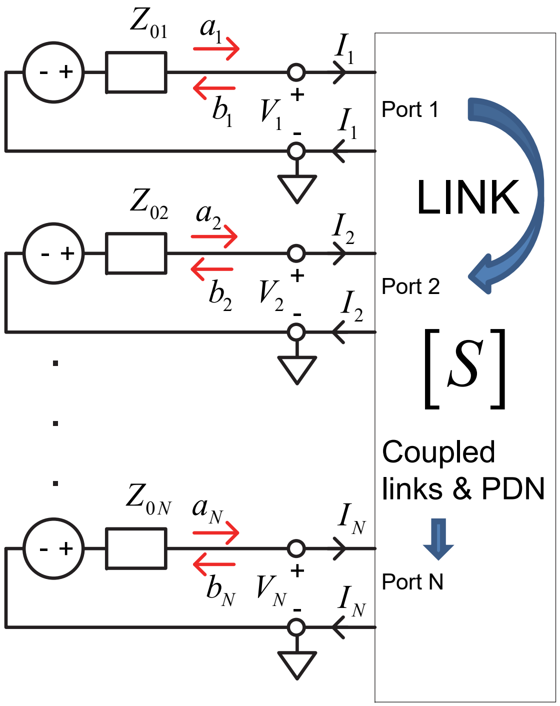
$P_{out} = \left|S_{2,1}\right|^2 P_{in}$

$\boldsymbol{P_{reflected} = \left|S_{1,1}\right|^2 P_{in}}$

$\boldsymbol{P_{dissipated} = \left(1 - \sum_k \left|S_{k,1}\right|^2\right) P_{in}}$

$P_{leaked} = \left(\sum_{k\neq 1,2} \left|S_{k,1}\right|^2\right) P_{in}$

$\boldsymbol{P_{coupled} = \left(\sum_{k\neq 1,2} \left|S_{2,k}\right|^2\right) P_{ink}}$



$\bar{a} = \frac{1}{2} Z_0^{-1/2} \cdot (\bar{V} + Z_0 \cdot \bar{I})$

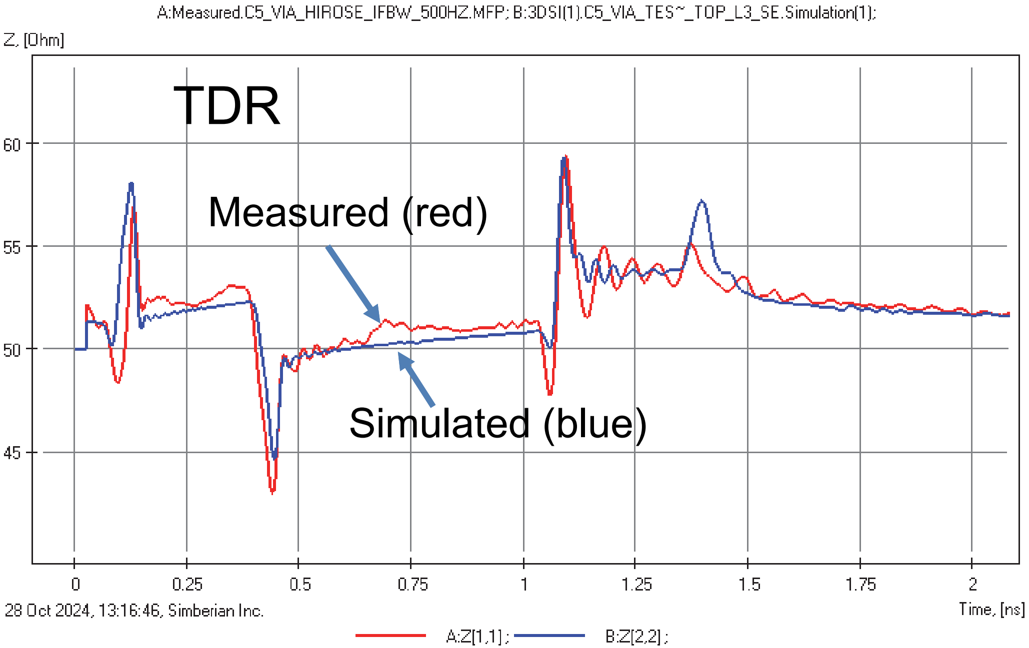
$\bar{b} = \frac{1}{2} Z_0^{-1/2} \cdot (\bar{V} - Z_0 \cdot \bar{I})$

$\bar{a}, \bar{b} \in C^{N\times 1}$
$Z_0 = diag\{Z_{0i}\} \in R^{N\times N}$

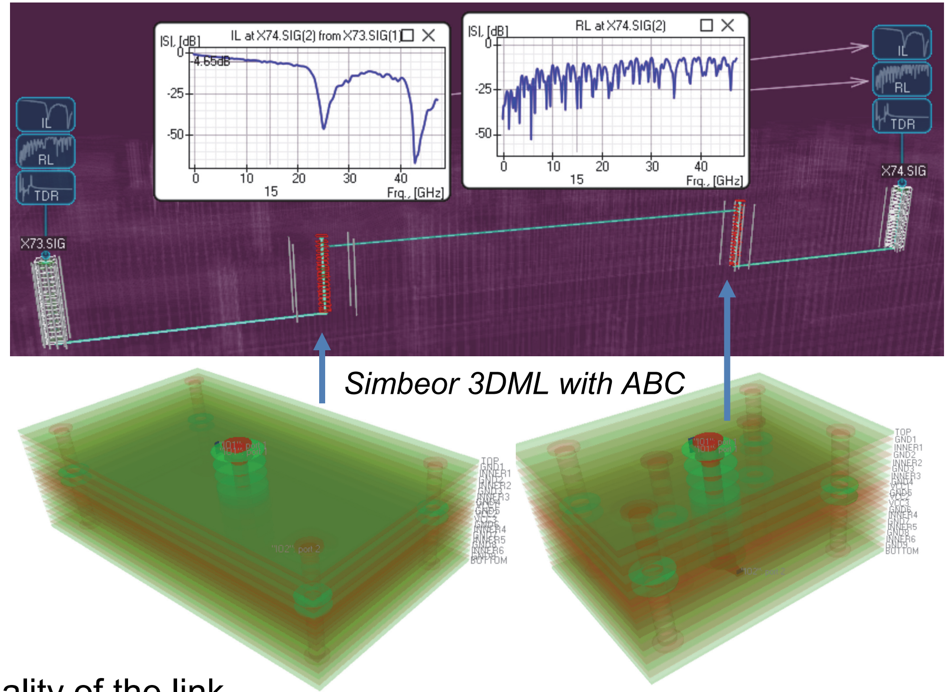
Scattering parameters:
$\bar{b} = S \cdot \bar{a} \quad S \in C^{N\times N}$

$S_{i,j} = \left.\frac{b_i}{a_j}\right|_{a_k = 0 k\neq j}$

Localized or Not?



C5 Structure from EvR-1 board (Expectation vs. Reality)



From TDR one can make erroneous conclusion on acceptable quality of the link…
Though, dips on IL and oscillations on TDR look strange – why? – absence of localization!

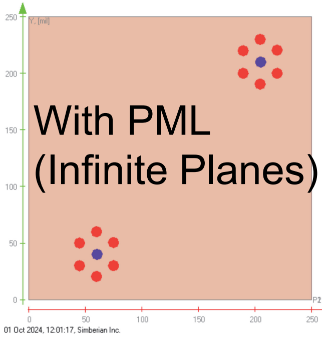
Localization and Distant Coupling – SE Vias

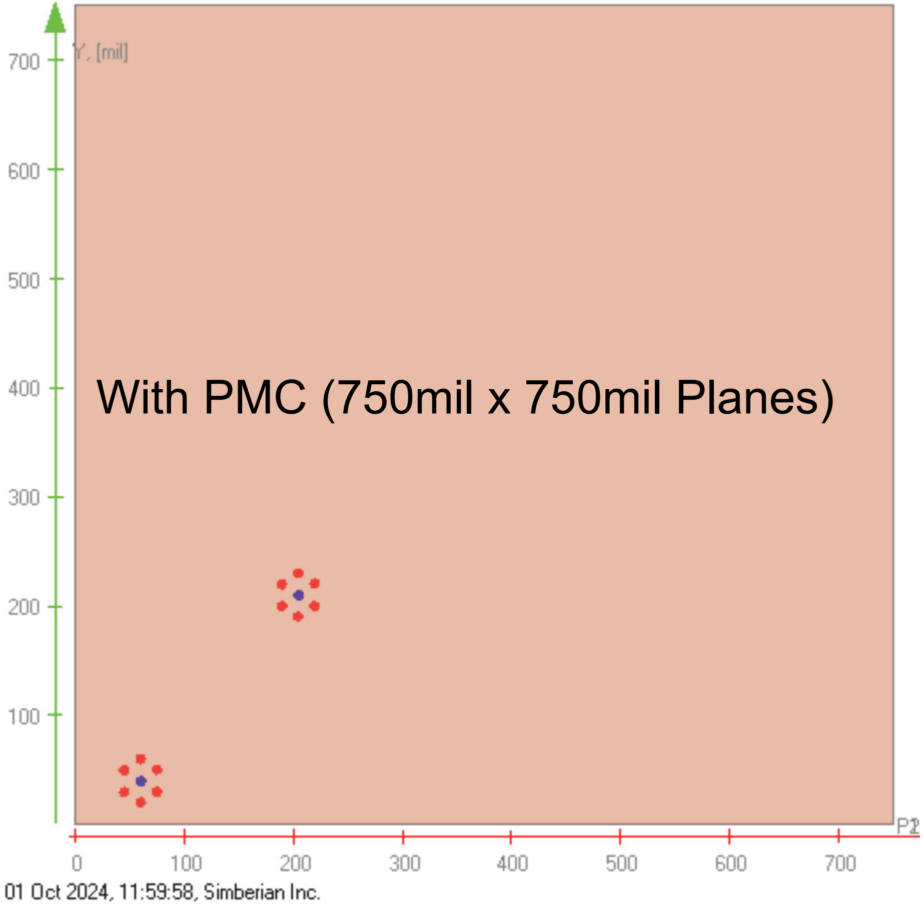
Two 0.77mil copper planes, separated by dielectric with Dk=3, LT=0.001

Two signal vias at 220mil (10mil diameter)
Number of stitching vias (Nstv) from 0 to 6 at about 20mil distance from signal

4-port structure with 50Ohm terminations

Physics-based model with 2D analysis in Simbeor 3DTF solver



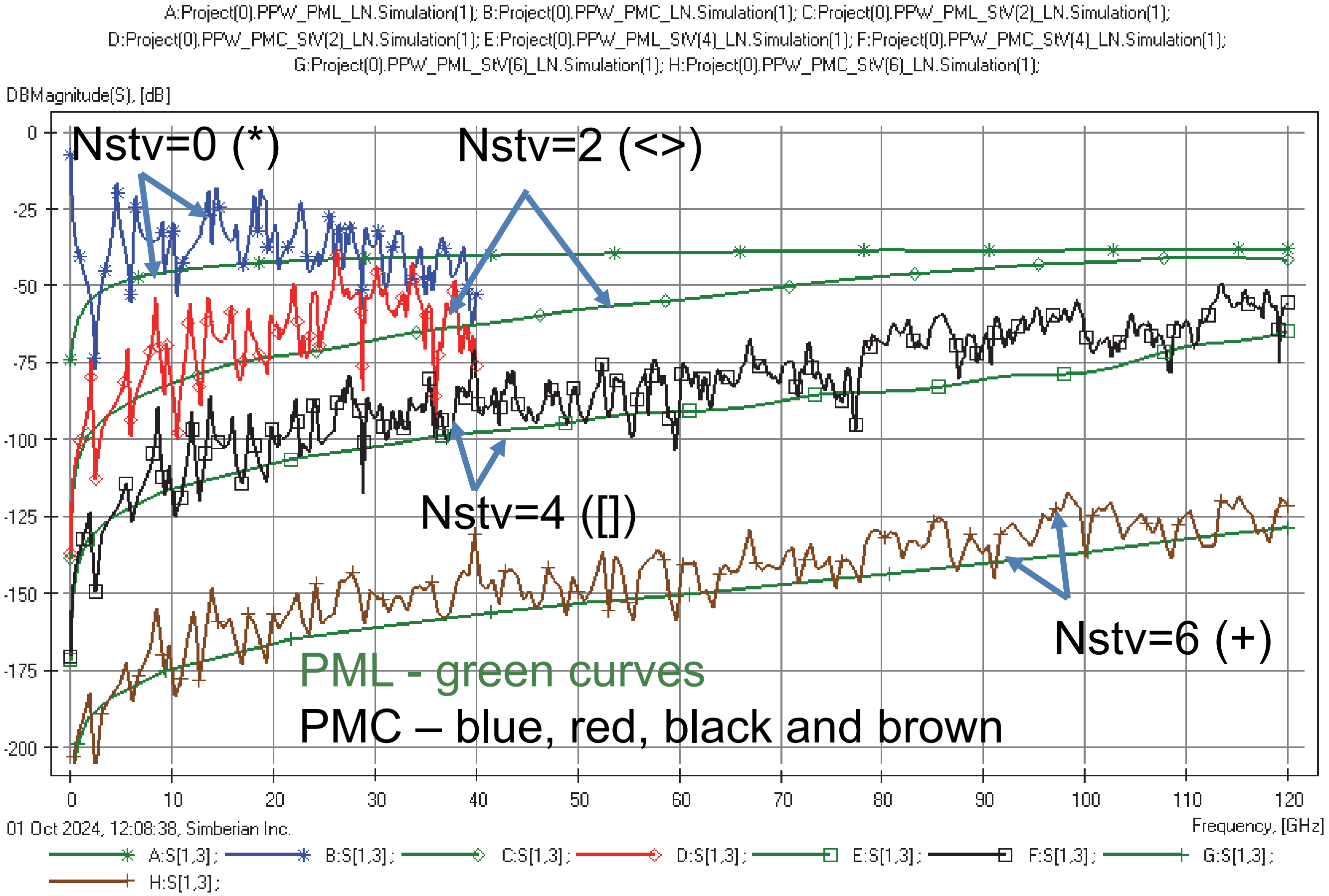


SE Vias Coupling with PMC and PML - H=2mil

750mil x 750mil with PMC and PML, increase of Stitching Count (Nstv) from 0 to 6

Coupling is reduced by increase of Nstv

Two stitching vias may be not enough



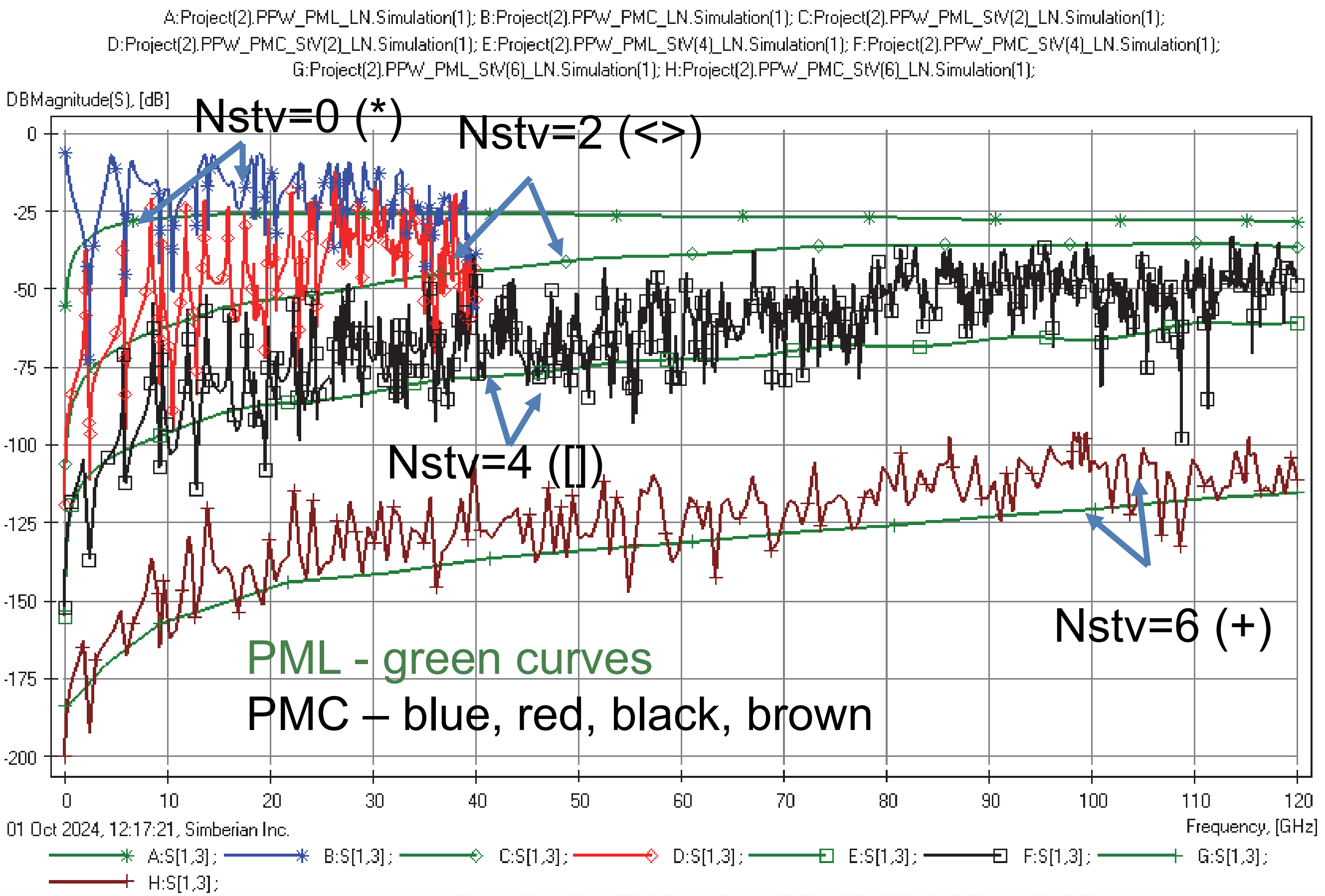
SE Vias Coupling with PMC and PML - H=20mil

750mil x 750mil with PMC and PML, increase of Stitching Count (Nstv) from 0 to 6

Coupling increases with plane separation

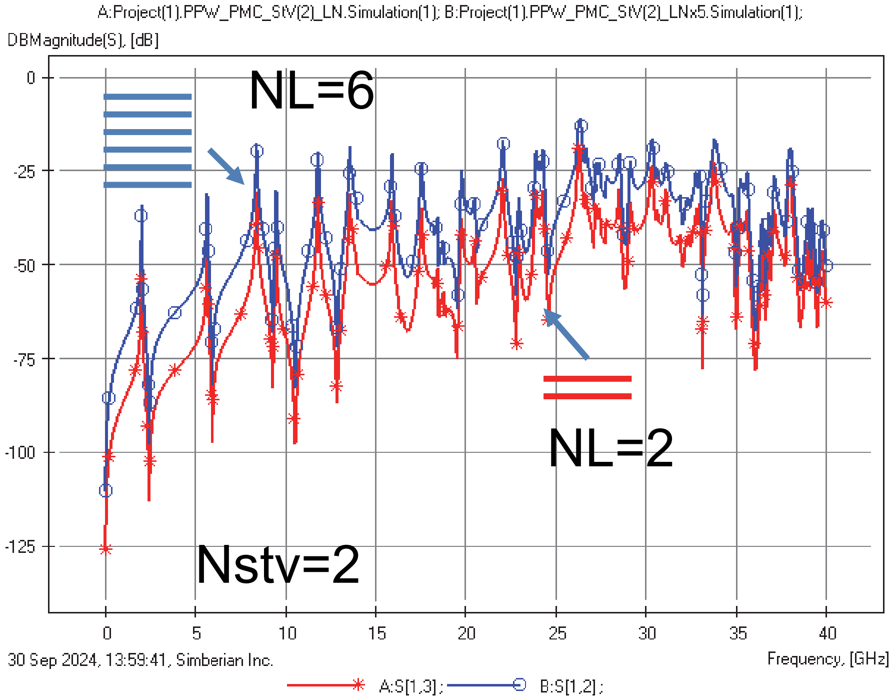
Coupling is reduced by increase of Nstv

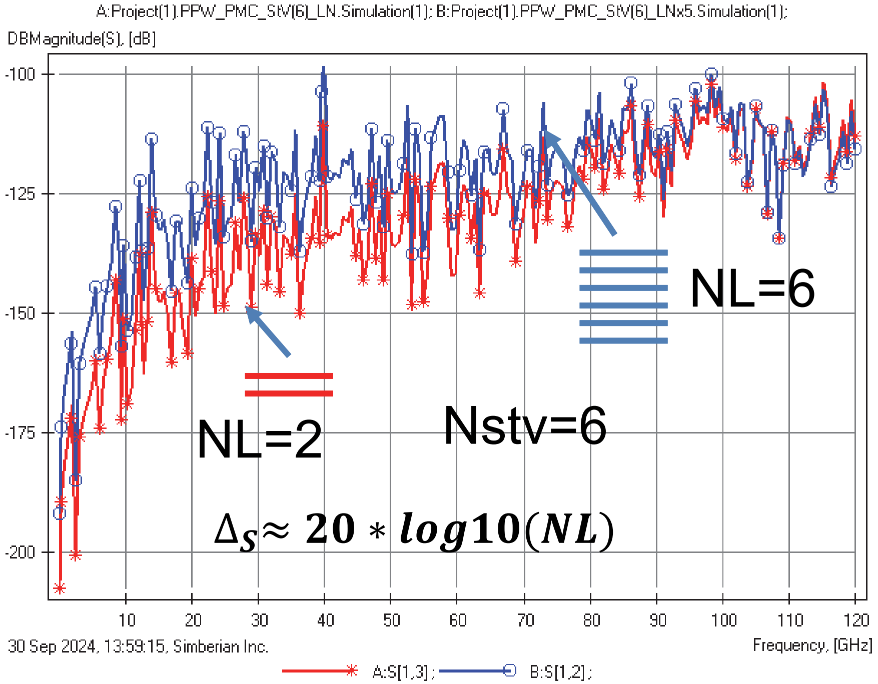
2 or 4 stitching vias is not enough



SE Vias Coupling Through Parallel Planes

750mil x 750mil with PMC, increase of Plane Count from 2 to 6 (H=9mil)

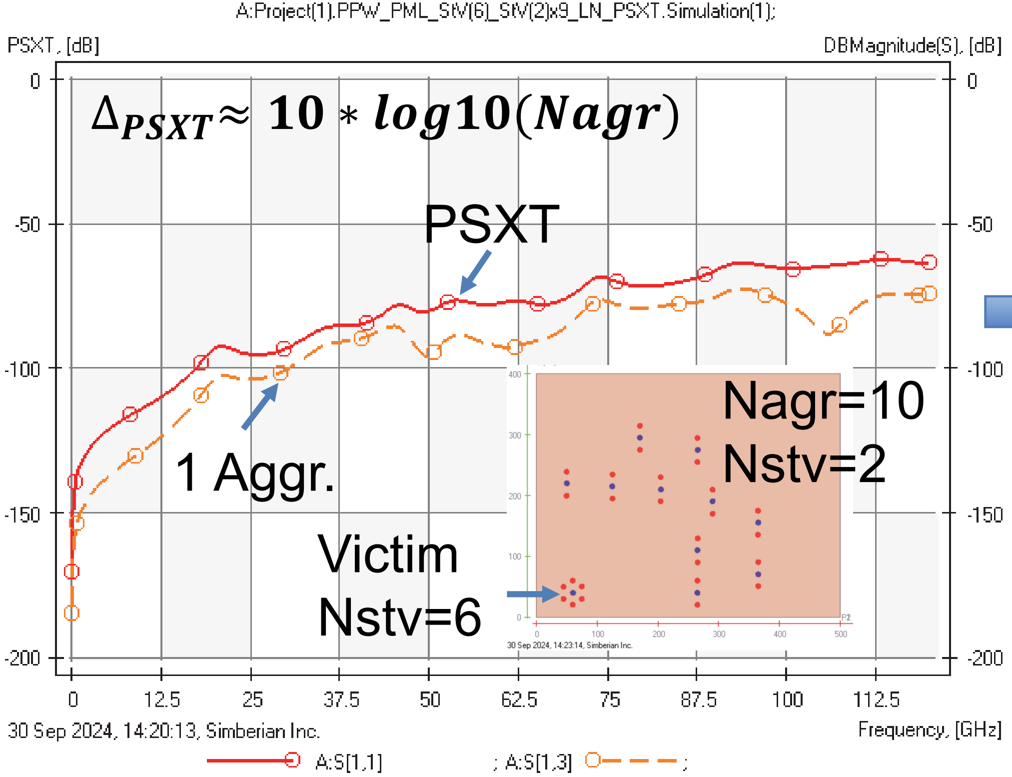


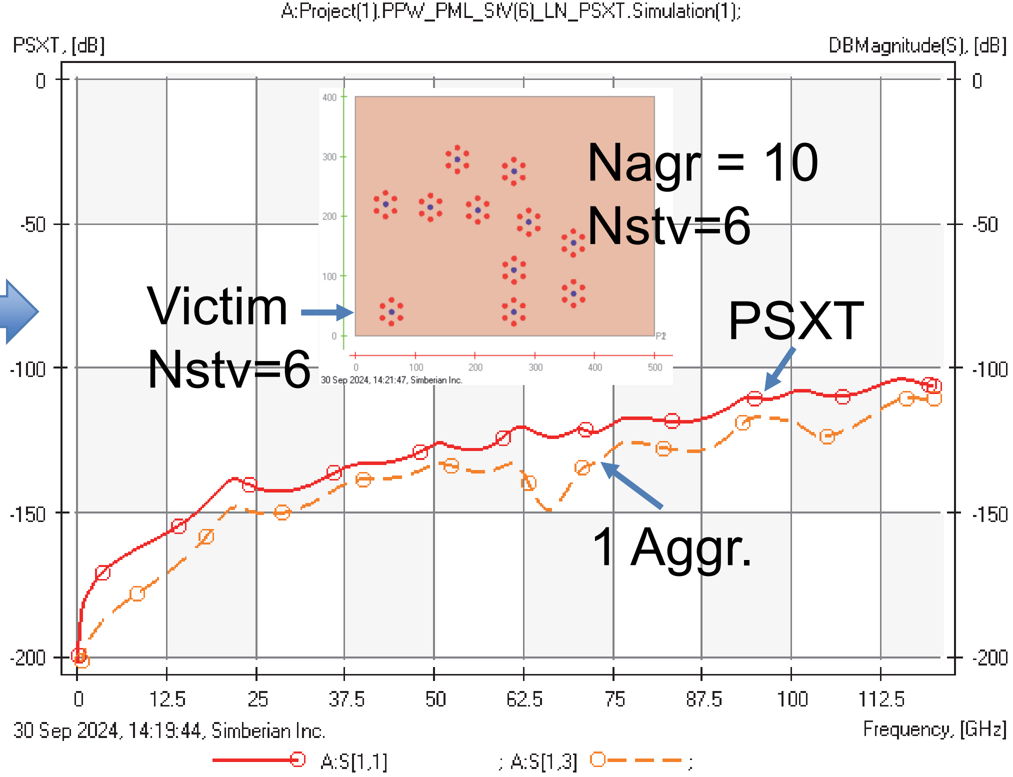


Multiple planes increase xtak, but stitching vias reduce it…

SE Vias Coupling Through Parallel Planes

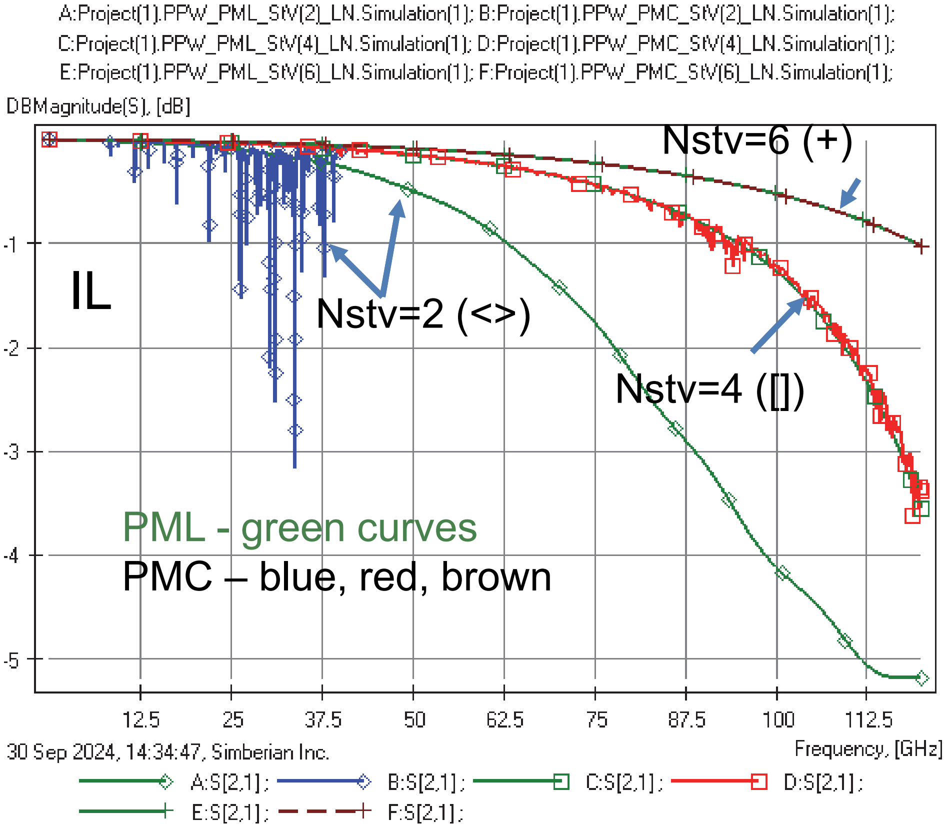
750mil x 750mil with PMC, increase of Aggressor Count from 1 to 10 (H=9mil)

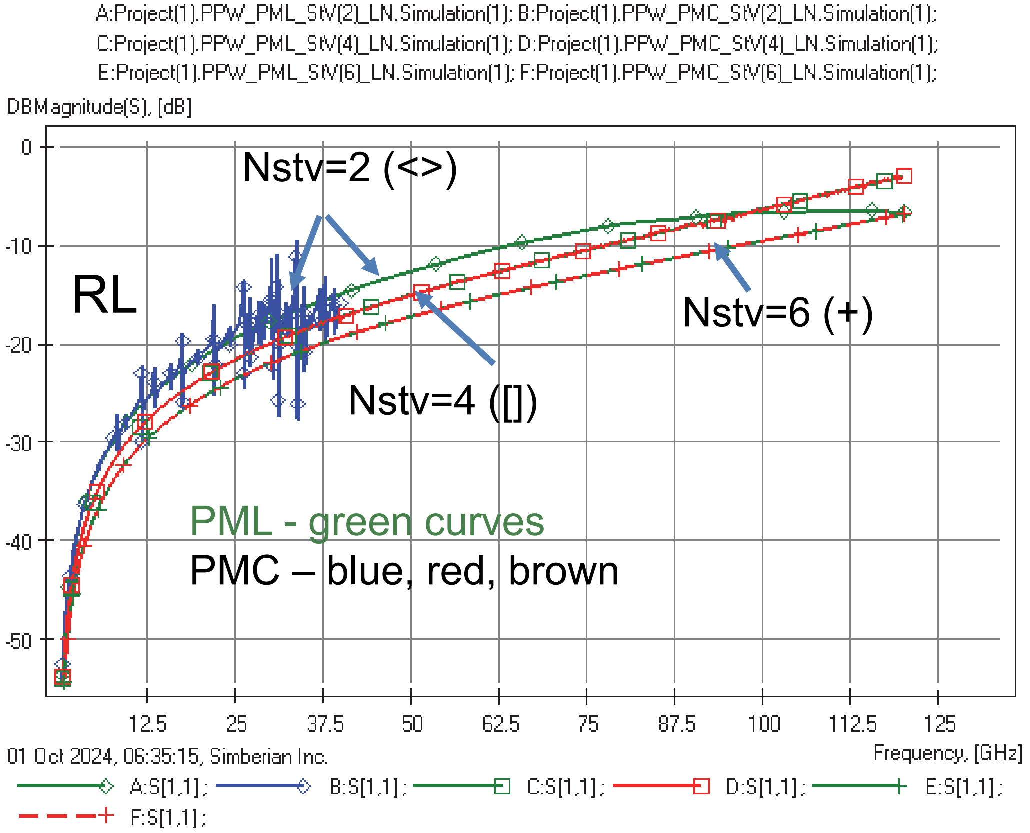




Multiple disturbers increase xtalk, but stitching vias reduce it…

Stitching Vias and IL & RL (H=9mil)

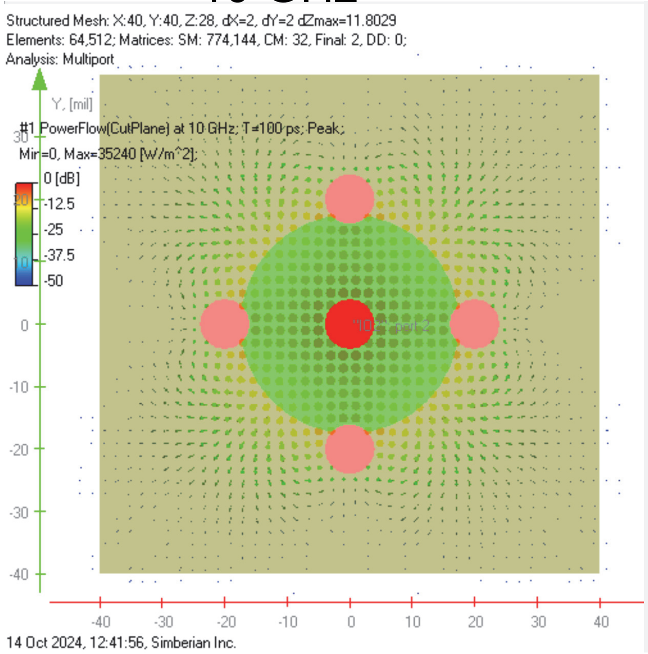




Coupling to cavities causes resonances in IL and RL, but stitching vias reduce it…

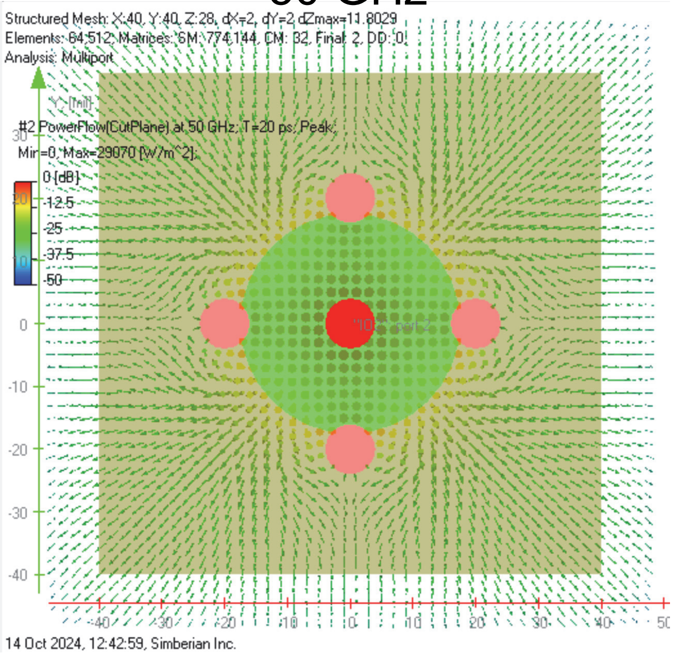
SE Via Power Flow Density, Nstv=4

10 GHz



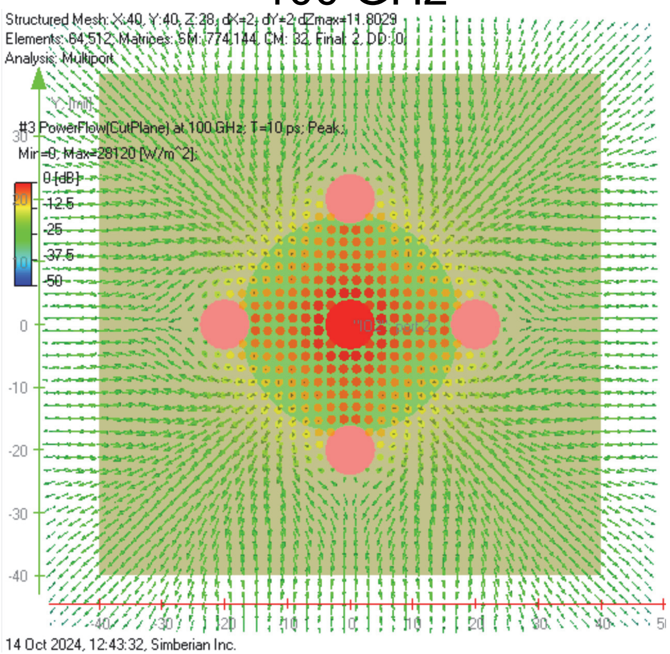
DP=0.24%

50 GHz



DP=1.7%

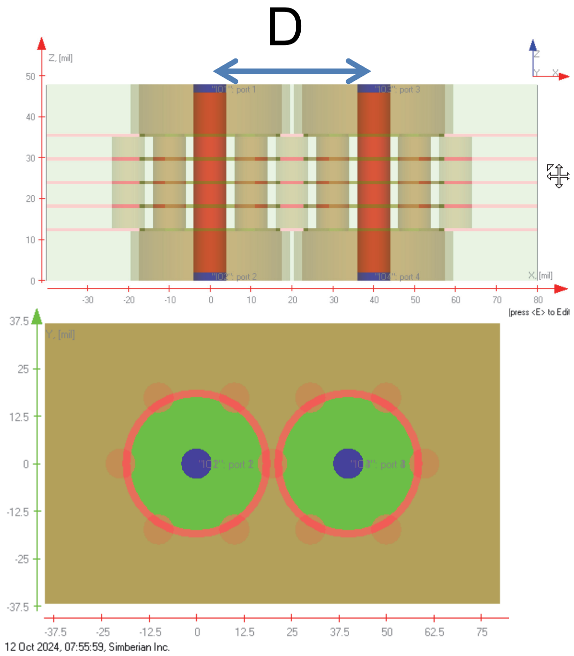
100 GHz



DP=11.4%

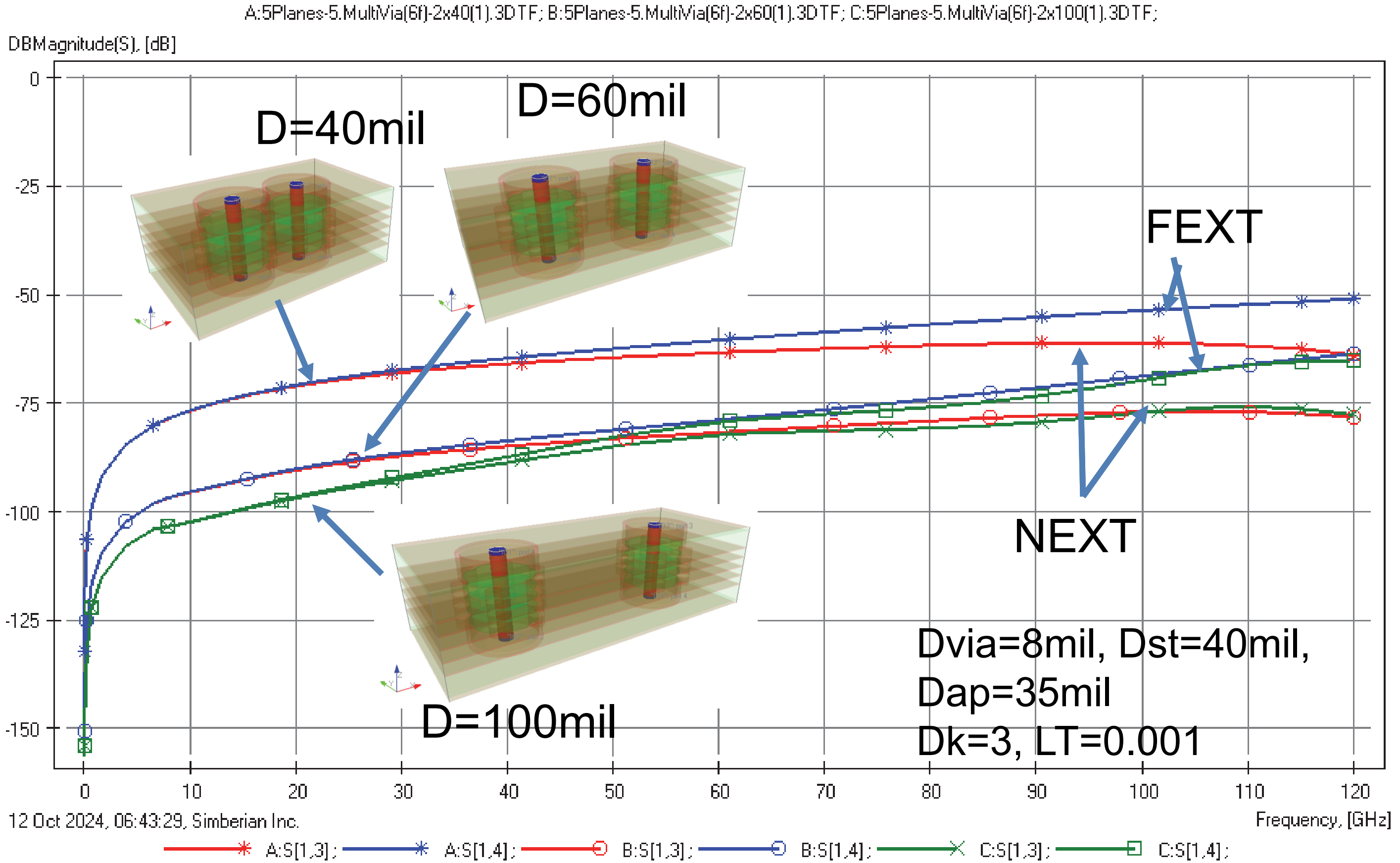
Peak PFD, Simbeor 3DTF, PML BC, Dvia=8mil, Dst=40mil, Dap=35mil, Dk=3, LT=0.001

Local Coupling – 3D EM, 5 planes, H=5mil

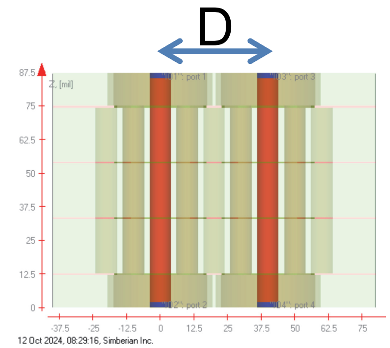


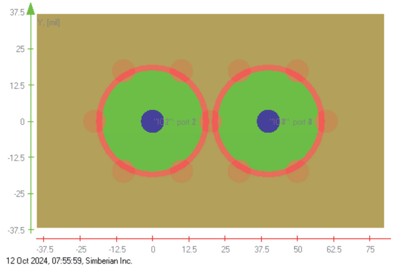
Dvia=8mil, Nstv=6, Dk=3, LT=0.001
Dst=40, Dap=35

Simbeor 3DTF, PML



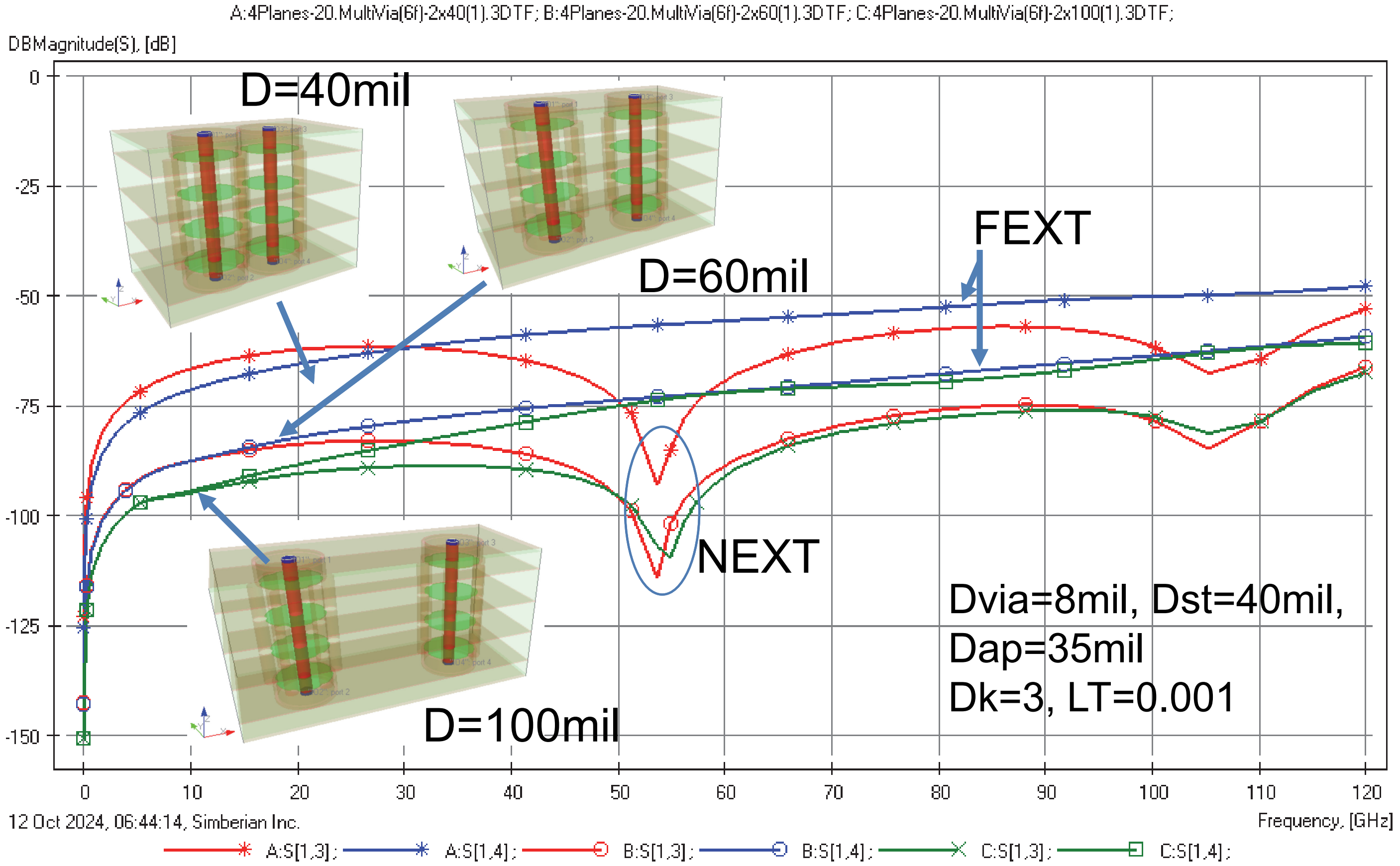
Local Coupling – 3D EM, 4 planes, H=20mil





Dvia=8mil, Nstv=6 Dk=3, LT=0.001
Dst=40, Dap=35

Simbeor 3DTF, PML



Localization and Distant Coupling – Diff. Vias

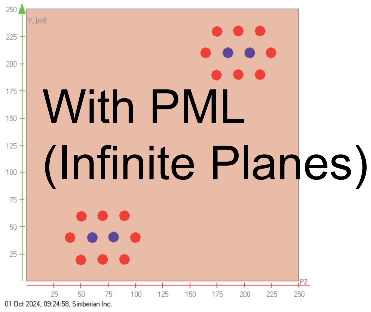
Two 0.77mil copper planes, separated by 9mil dielectric with Dk=3, LT=0.001

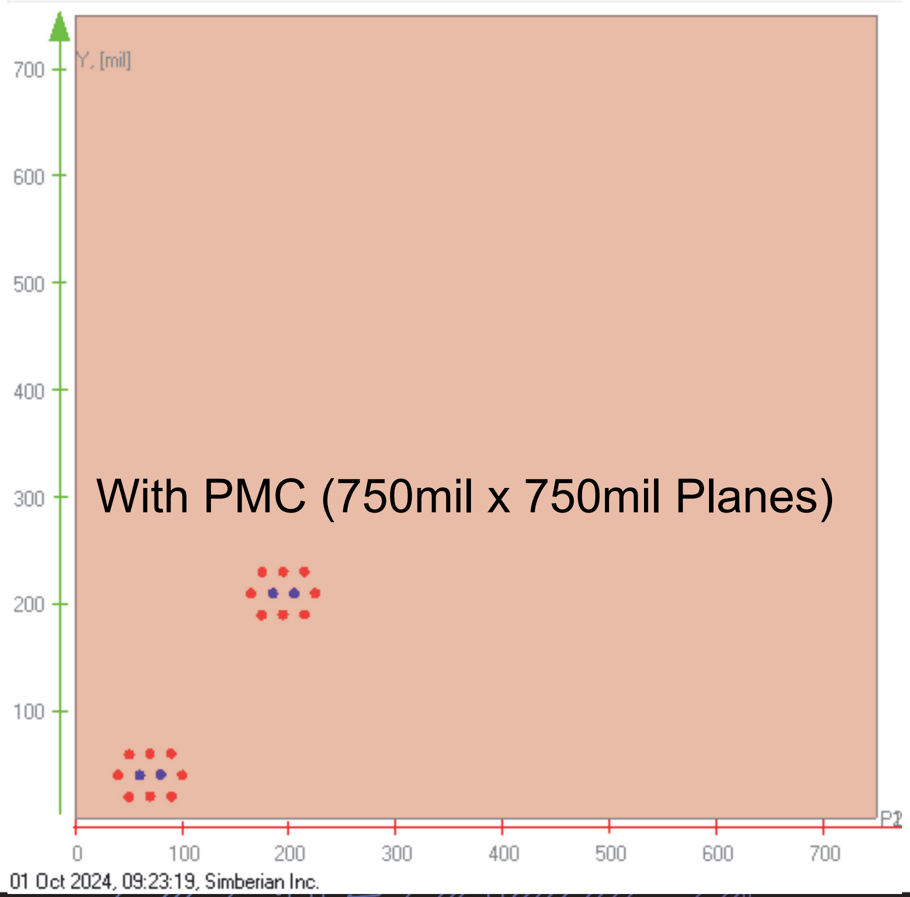
Differential signal vias 20mil distance (10mil diameter), two pairs at ~220mil

Number of stitching vias (Nstv) from 0 to 8 at about 20mil distance from signal

8-port structure with 50Ohm terminations

Physics-based model with 2D analysis in Simbeor 3DTF solver



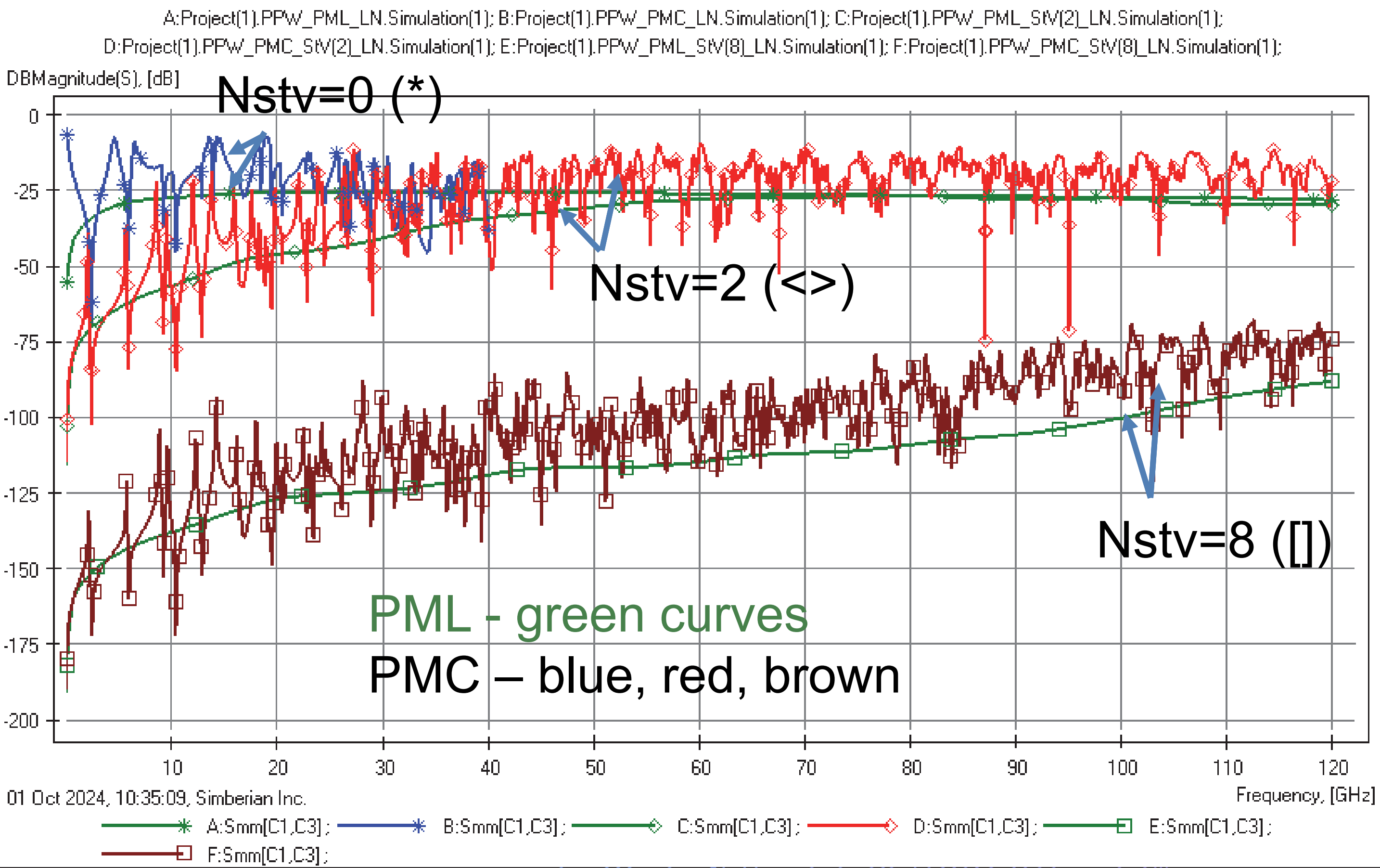


Common Mode Coupling in Diff. Vias

CM coupling is reduced by increase of Nstv (similar to SE)

Two stitching vias is not enough

If CM isolation is needed – more stitching vias is required

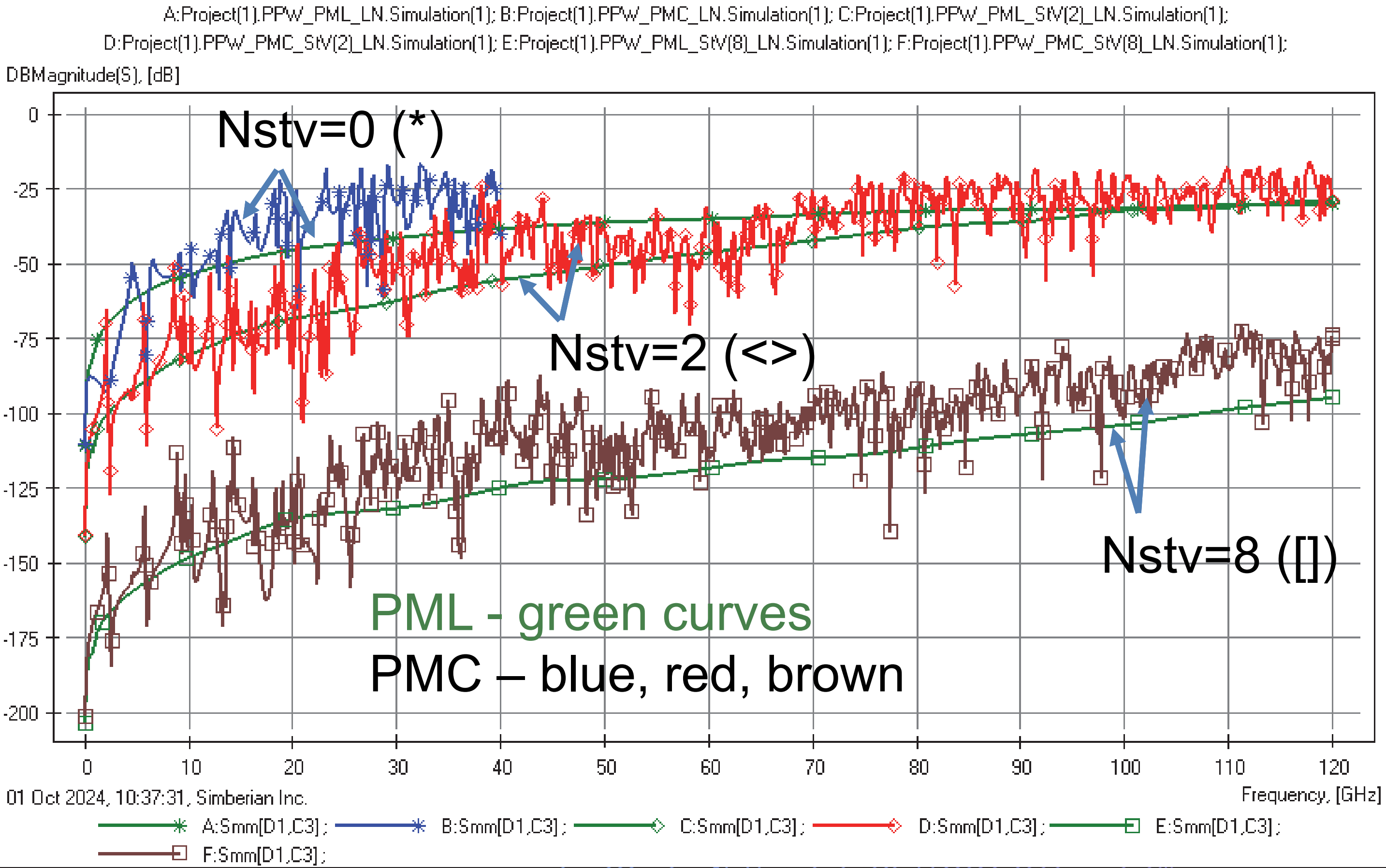


Common to Differential Mode Coupling

Modal coupling through PDN even in symmetrical vias

Depends on PDN geometry and resonances

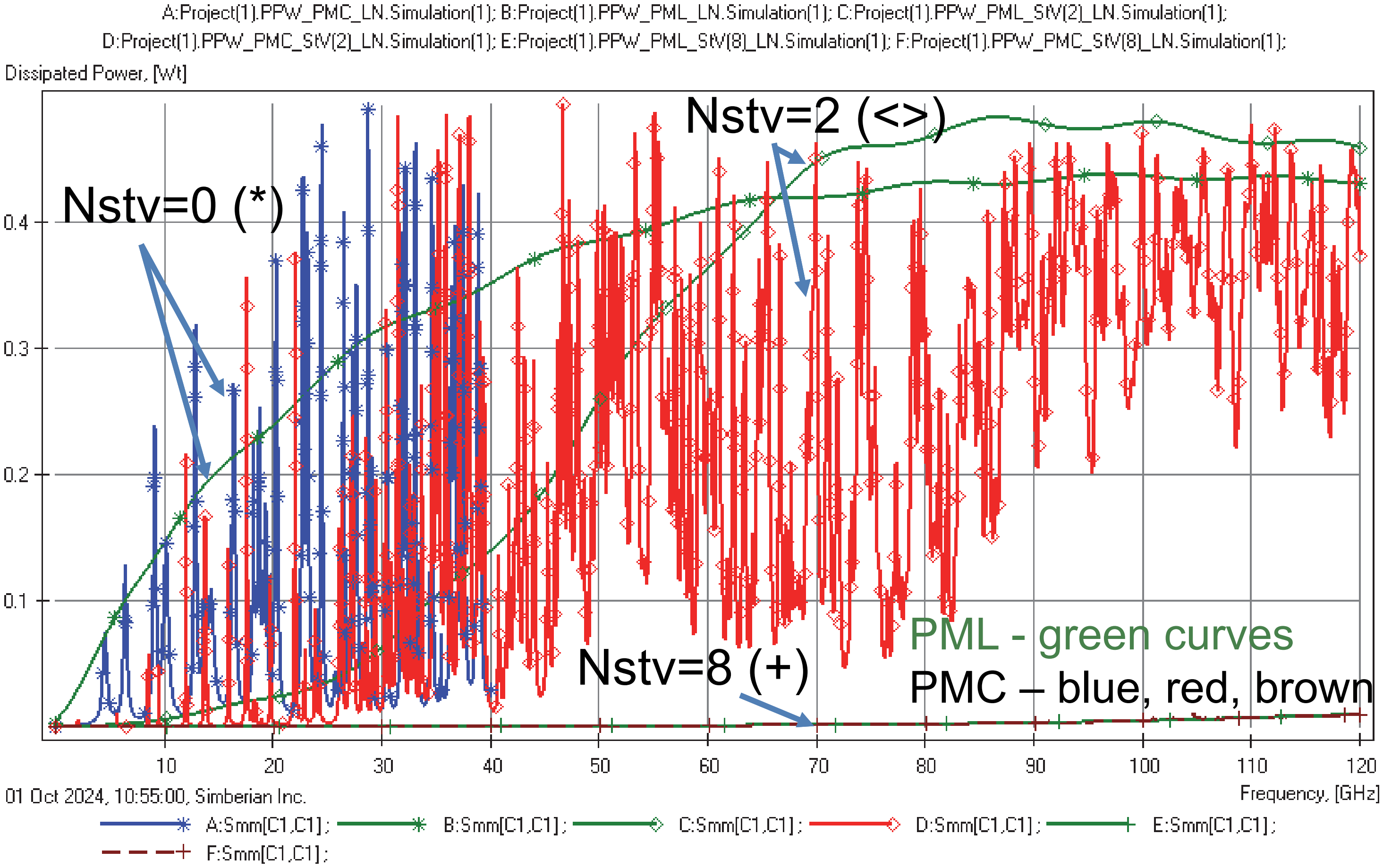
It is reduced by increase of Nstv



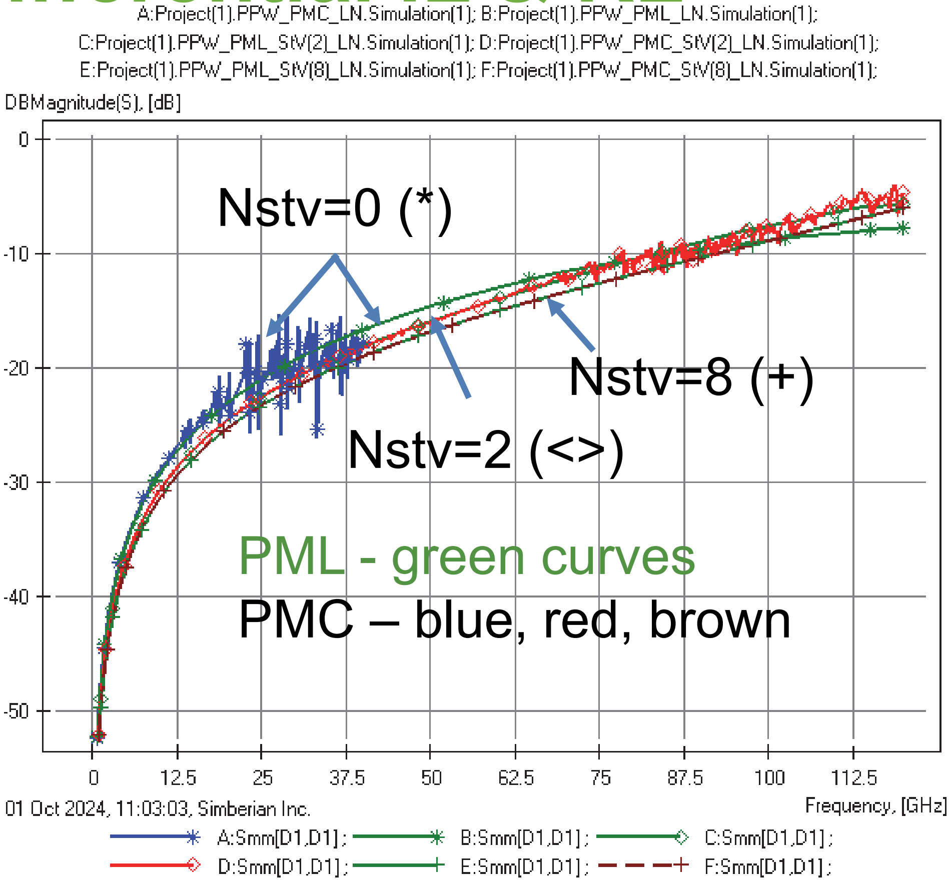
Common Mode Dissipated Power

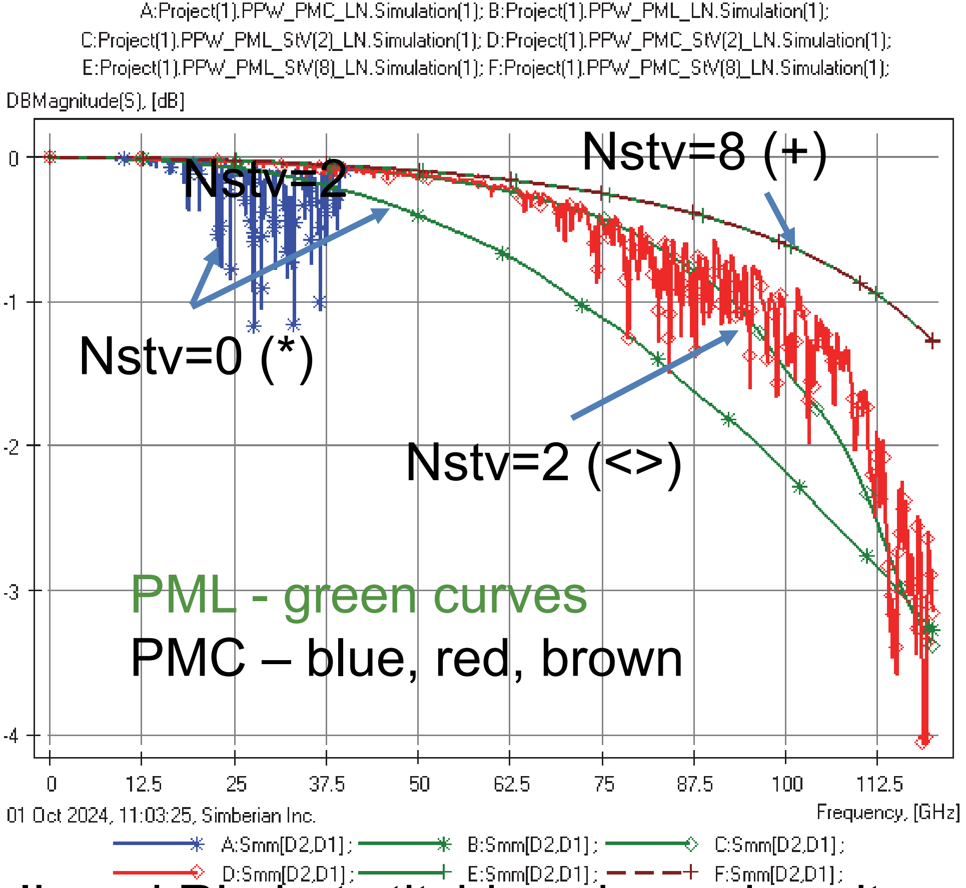
Stitching vias reduce leaks of common mode

Require more stitching vias for ideal de-coupling from PDN



Differential IL & RL

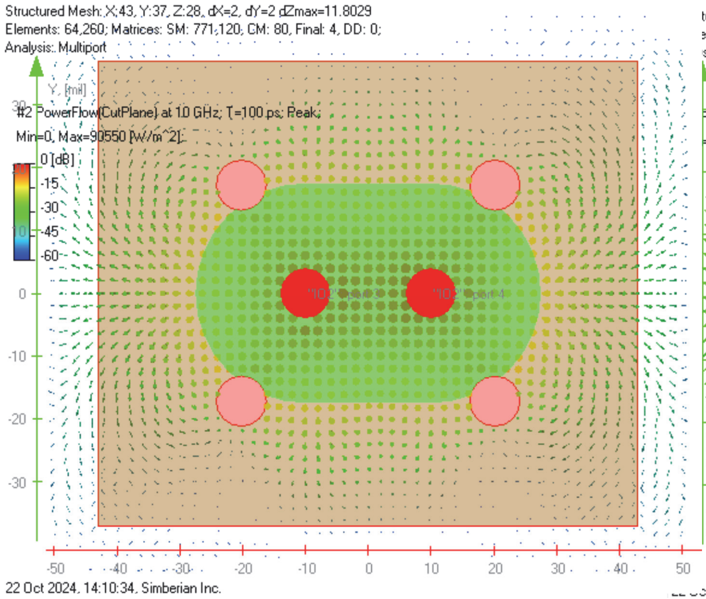




Coupling to cavities causes resonances in IL and RL, but stitching vias reduce it…

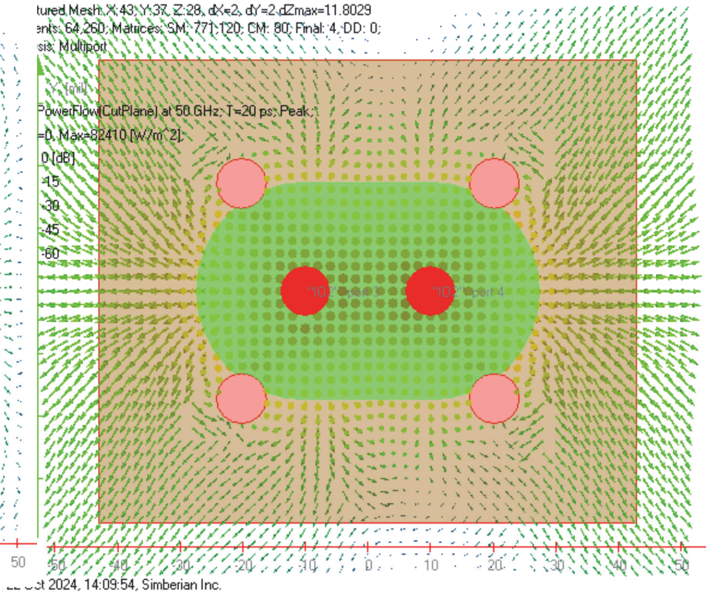
Diff. Vias Power Flow Density, Nstv=4

10 GHz



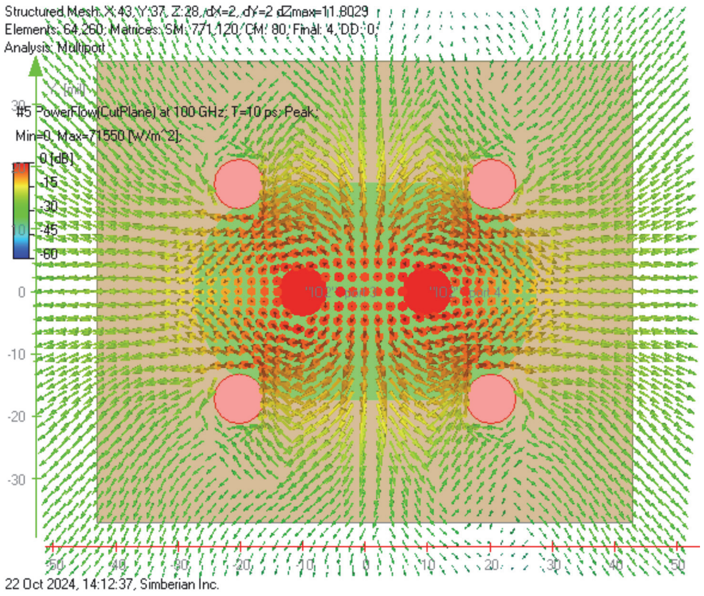
DP=0.14%

50 GHz



DP=1.6%

100 GHz



DP=14%

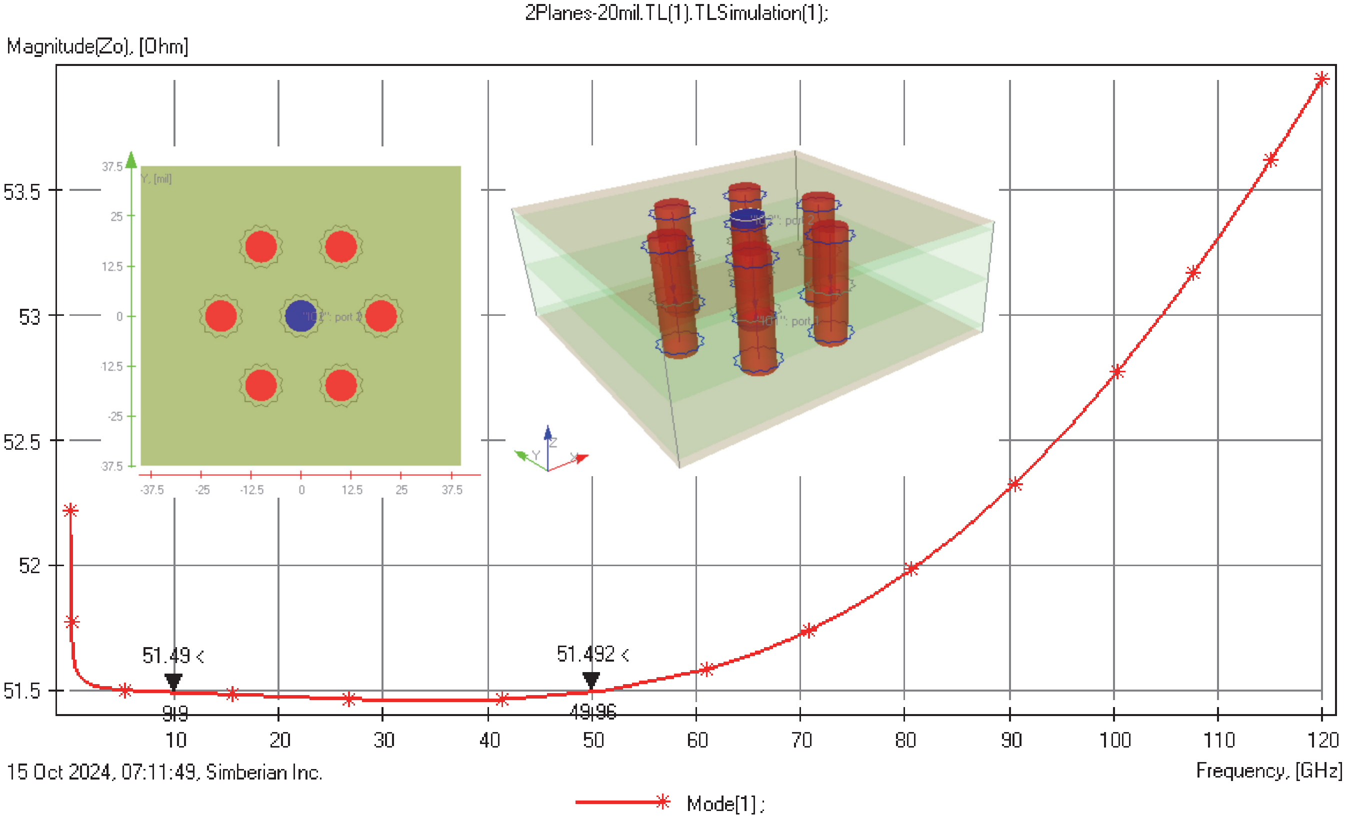
Peak PFD, Simbeor 3DTF, PML BC, Dvia=8mil, Dvv=20mil, Hap=35mil, Dk=3, LT=0.001

Middle Section Design as SICW

Nstv=6, Dvia=8mil, Dstv=40mil

Dk=3, LT=0.001

Zo is higher than the target 50 Ohm in anticipation of additional plane capacitance

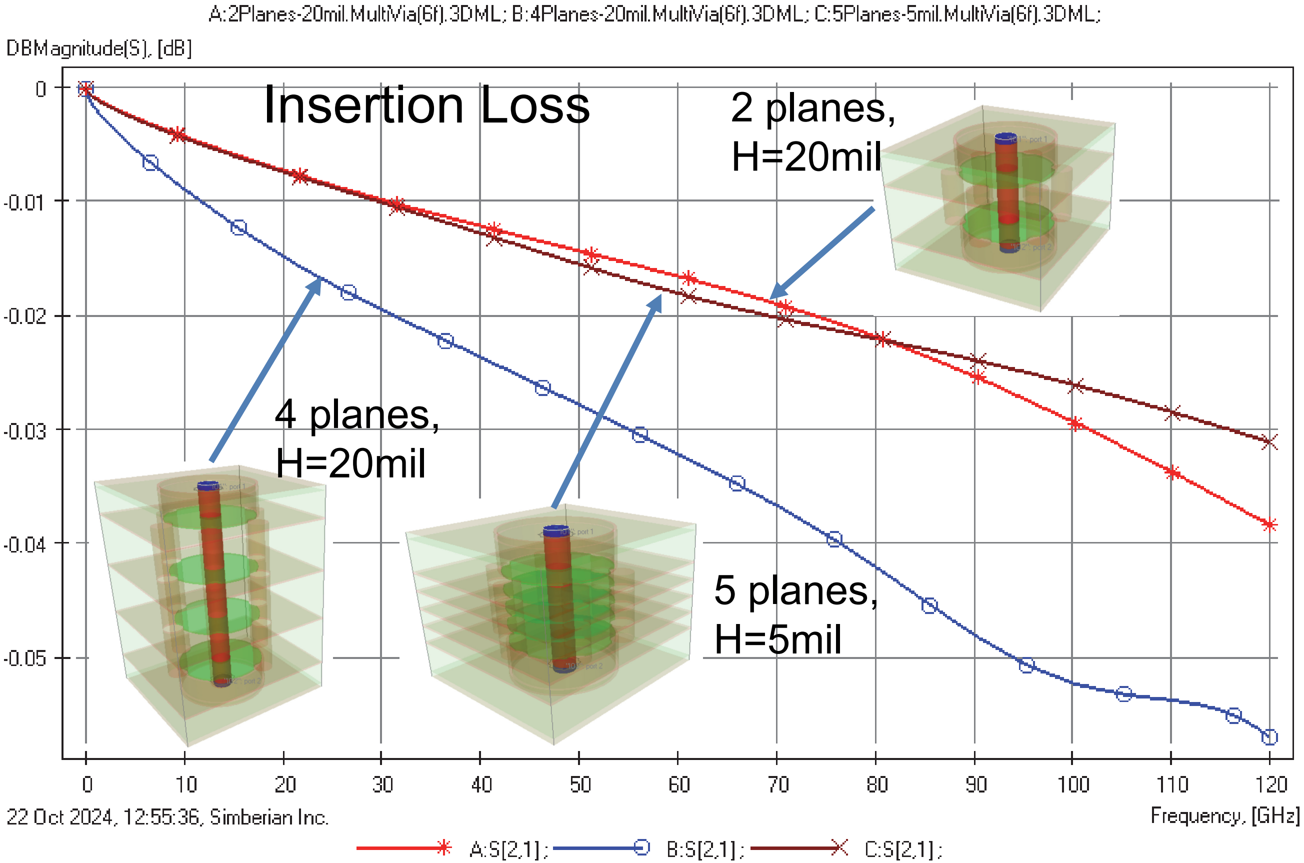


IL of SICW

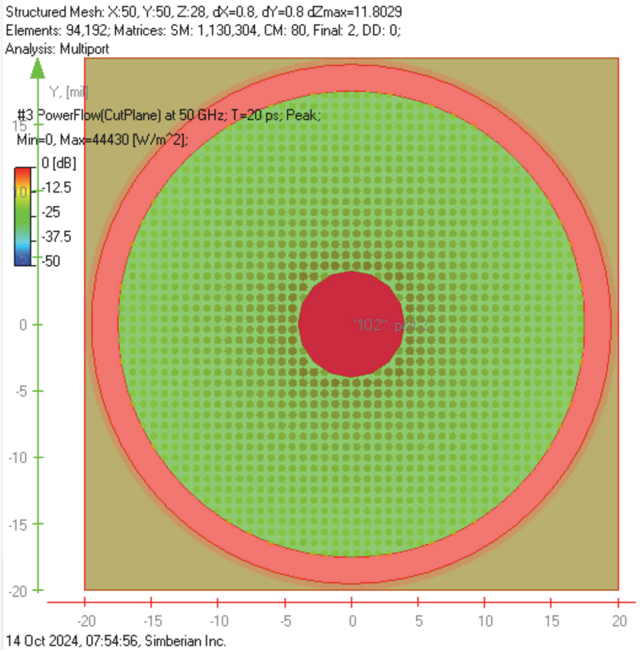
Immune to stackup structure changes

Nstv=6, Dvia=8mil, Dst=40mil, Dap=35mil
Dk=3, LT=0.001

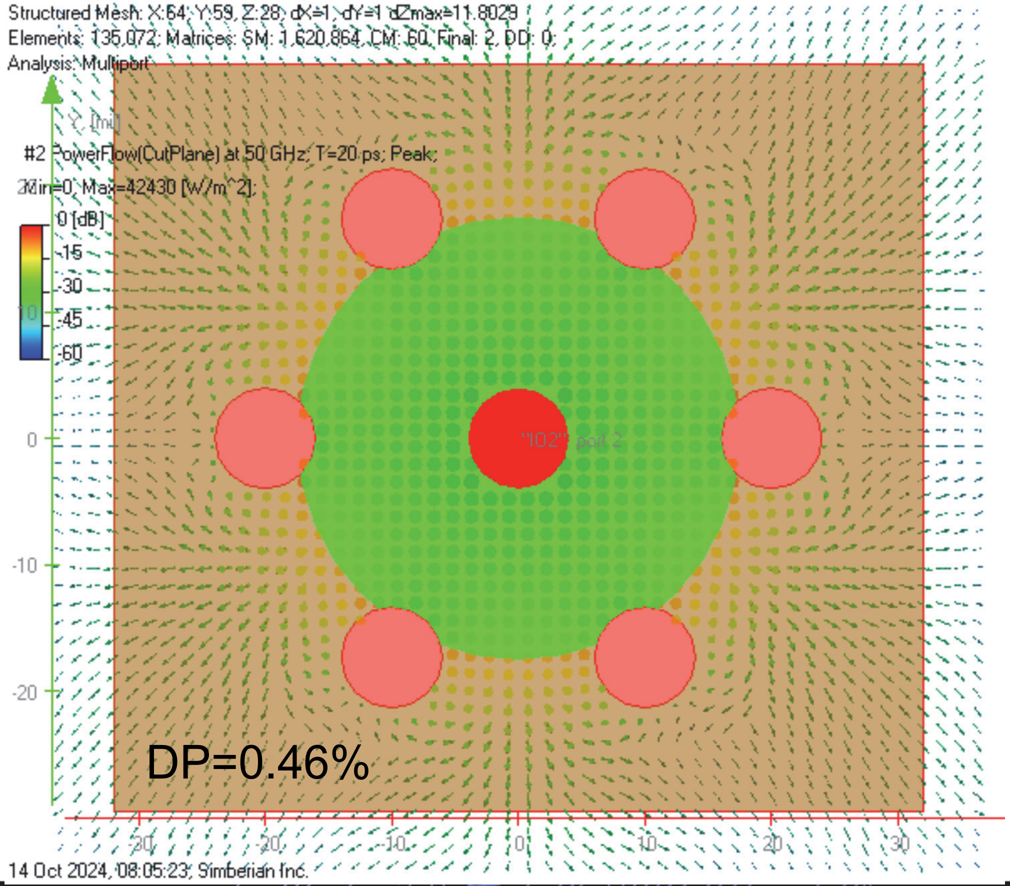
Simbeor 3DML, ABC



Power Flow Density in SICW at 50 GHz



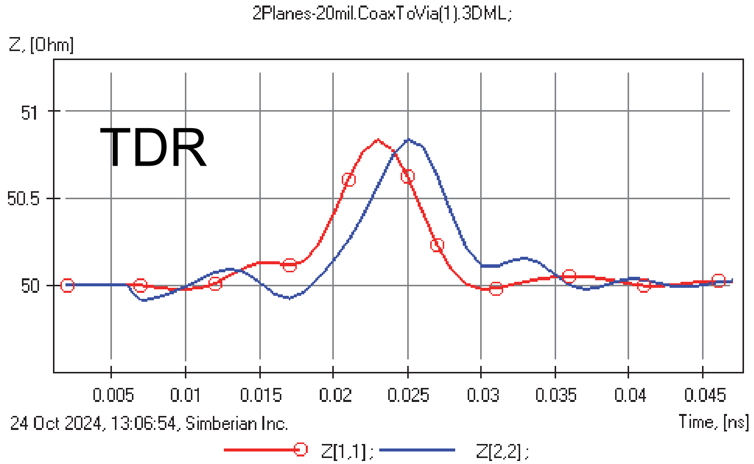
DP=0.42%

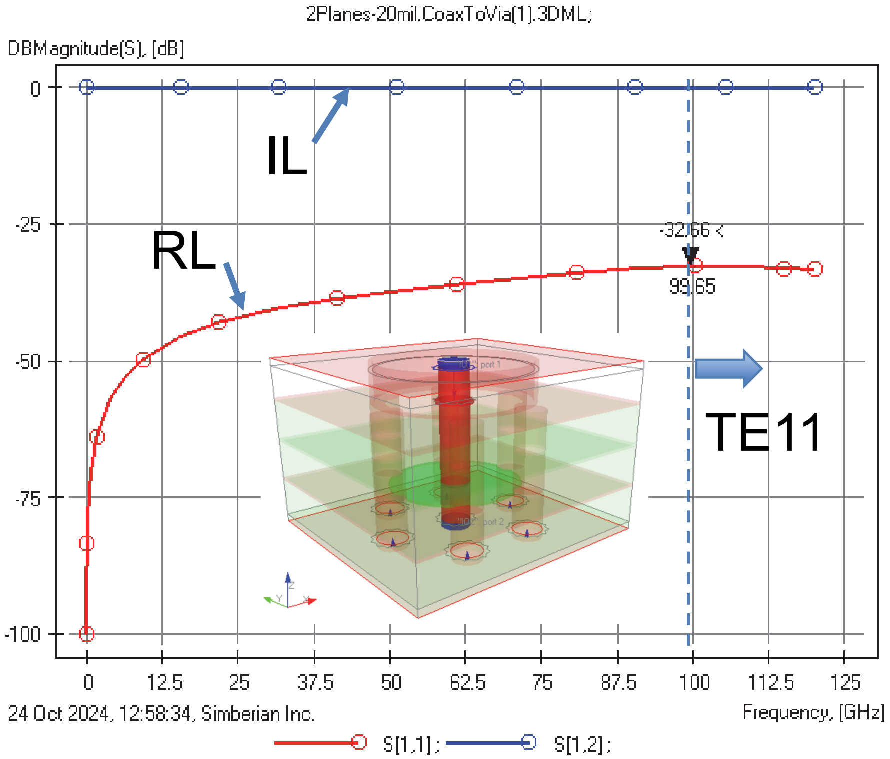


DP=0.46%

SE Via Vertical to Vertical Transition (VVT)

Coaxial to SICW – match impedance and cross-section as possible

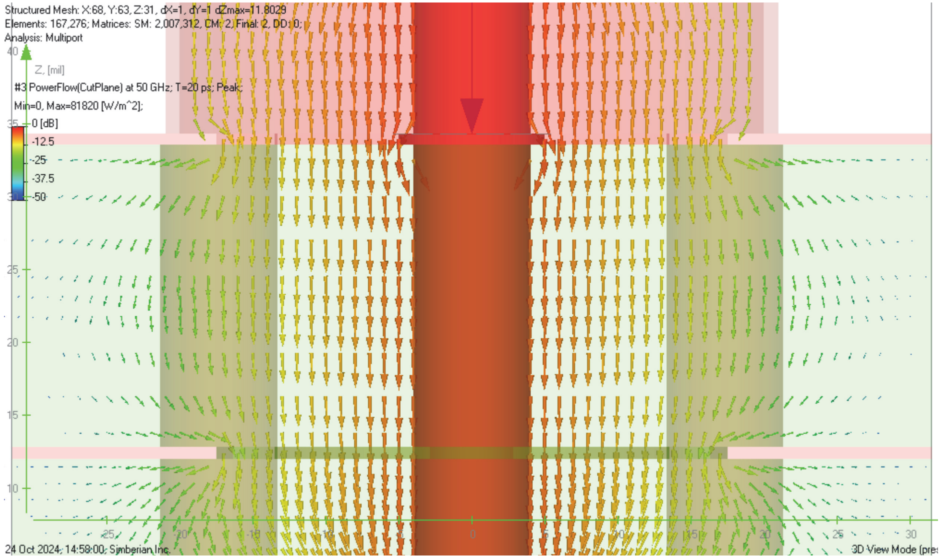




SE Via VVT – Power Flow Density

Maintain impedance continuity and minimize discontinuities:
Provide continuous Power Flow from Coax to SICW

Peak PFD at 50 GHz



Peak PFD at 100 GHz