Waveguiding Approach to Via Design with Bandwidth over 120 GHz

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Abstract — **In this paper, we introduce a novel approach to the design and optimization of PCB and packaging vias for high-speed applications with bandwidths over 120 GHz. We propose the design of any-stackup vias using waveguiding structures similar to substrate-integrated waveguides, specifically substrate-integrated coaxial (SICW) and twinax (SITW) waveguides. This design is further simplified by segmenting the vias into middle sections and transitions. Our analysis demonstrates that the middle sections of SICW and SITW are relatively independent of the stackup structure and insensitive to the number and location of reference planes. Our work provides a robust and simple methodology for designing vias that are less sensitive to manufacturing variations and stackup adjustments and suitable for bit rates up to 448 Gbps.**

I. Introduction

Designing PCB and packaging interconnects for 224–448 Gbps presents multiple challenges, with vertical transitions, or vias, being among the most critical. Vias can dissipate and reflect signals, contributing to crosstalk noise through both local and distant coupling to other links.

Via analysis and optimization are primarily driven by 3D electromagnetic modeling [1]-[7]. Such analysis is typically applied to a relatively small area around single-ended or differential vias with stitching vias to evaluate reflection, transmission, and possible local coupling. However, 3D EM analysis does not guarantee via model accuracy, as it largely depends on via localization. The behavior of unlocalized or poorly localized vias is unpredictable when simulated in isolation using practically any type of 3D EM analysis [7].

Regarding via design techniques, the mainstream approach is direct optimization using 3D EM solvers [2]-[5], [7]. However, indiscriminate optimization of all via parameters may result in complex structures that are highly sensitive to manufacturing variations and require excessive computational effort and design resources. Simultaneous direct optimization of vias across different layers simplifies design and enables the use of a common padstack for multiple layers [3]. Additional design simplifications can be achieved using domain decomposition [6], [7]. This paper adopts this approach as an alternative to simultaneous optimization. The middle section design is further simplified by transforming it into a segment of a substrate-integrated waveguiding structure with very low sensitivity to antipad misregistration and dielectric constant variations.

II. Via Design Goals and Approach

The primary goal of via design is typically to reduce reflection across the signal bandwidth or in time domain (TDR). Another key objective is minimizing crosstalk by improving via localization, enabling simulation independent of the rest of the PCB. As shown in [7], localization can be formally evaluated through comparative analysis of power dissipated in a via simulated with PML boundary conditions.

Additional via design challenges stem from manufacturing considerations. PCB manufacturers adjust designs based on available laminates and supported fabrication methods, leading to variations in materials and stackup dimensions. Consequently, ideally designed low-reflection vias may exhibit unacceptable reflections when stackups are modified - a factor that often becomes apparent only at the post-layout stage. These uncertainties reduce design margins. To address this, we introduce a new approach for designing vias that are less sensitive to stackup adjustments and manufacturing variations, such as layer misregistration.

The via design goals proposed in [7] can be summarized as follows:

- **Ensure localization and single-mode bandwidth up to 1.5x - 2× the Nyquist frequency.**
- **Maintain reflections below a defined threshold.**
- **Reduce sensitivity to manufacturing variations.**
- **Ensure usability across different layers.**

To avoid redesigning vias for each layer, domain decomposition can be employed [6], [7]. A via is divided into a reusable middle section and either a vertical-to-horizontal transition (VHT) for via-to-trace connections or a vertical-to-vertical transition (VVT) for via-to-connector or via-to-BGA sections. Each section can be independently designed with appropriate waveguiding ports at their boundaries.

To ensure the middle section is compatible across layers, the via must closely resemble a transmission line or waveguiding structure. The next two chapters introduce new waveguiding via designs for single-ended and differential cases.

III. Substrate Integrated Coaxial Waveguide

One way to convert a single-ended via into a waveguiding structure is to design it as a coaxial waveguide. This approach was suggested in [8], but it lacked essential constraints on antipads. Here, we propose constructing a coaxial via similar to a substrate-integrated waveguide (SIW) [9], referred to as a Substrate Integrated Coaxial Waveguide (SICW).

First, the outer conductor of the coaxial structure is replaced by stitching vias. Equations defined for coaxial waveguides (CW) and SIW can be used to determine the dimensions of SICW, as shown in Fig. 1. Second, setting the antipad diameter equal to the effective coaxial waveguide diameter (D) transforms the via into a waveguiding structure that is largely independent of the planes.

$$D = d \cdot e^{2\pi Z_o \sqrt{\frac{\varepsilon}{\mu}}}$$

$$s < 0.4\lambda \quad D_{ap} \approx D$$

$$Dst = D + \frac{d^2}{0.95 * s}$$

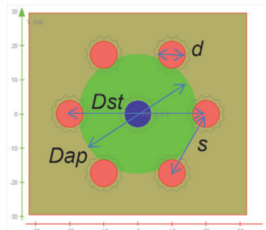

Fig. 1. SICW design equations – d and D are inner and outer diameters of coaxial waveguide with impedance Zo.

The localization of SICW depends on the number of stitching vias Nstv and distance between them s. As recommended for SIW [9], s should be smaller than 0.4 of wavelength in dielectric λ, to reduce the leaks. However, the localization should be also verified with the dissipated power metric, that is usually more restrictive condition [7] (requires more stitching vias). The effective coaxial diameter D, computed as shown in Fig. 1, approximately defines the cutoff frequency $f_{cutoff} \approx \frac{2c}{\pi(d+D)\sqrt{\varepsilon}}$ for the first high order mode. The cutoff frequency defines the single-mode bandwidth of the SICW. For instance, it is 96.4 GHz (suitable for 224 Gbps) for SICW with dielectric constant Dk = 3, via diameter d=8mil, stitching ring diameter Dst=40mil, stitching via count Nstv=6, and distance s=21mil. Note that via is localized even above 96 GHz, but it will be not functional as we will see in the analysis of via transition to strip line. To increase the bandwidth, the SICW should be reduced in size. For instance, for Dk = 3, d=4mil, Dst=20mil Nstv=8, s=7.8mil, the TE11 cutoff frequency is about 199 GHz, that is suitable for data rates up to 448 Gbps.

To evaluate sensitivity of SICW, we use analytical expression for coaxial waveguide impedance Z_o. Change of impedance due to change in dielectric constant $\Delta\varepsilon$ can be expressed as follows: $\Delta Z_o \approx -\frac{\Delta\varepsilon}{2\varepsilon} * Z_o$. 10% change in ε or Dk produces only about 5% change in the impedance (equivalent to -32dB in RL). Considering the effective coaxial diameter D that is also equal to the antipad size, small change ΔD cause the following change in impedance: $\Delta Z_o \approx \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * \frac{\Delta D}{D}$. The sensitivity to this parameter is also relatively small, because of large D. For instance, 1mil change in D=40mil can cause only 1 Ohm change in the impedance (equivalent to -40dB in RL). Finally, change in via diameter Δd changes the via impedance as follows: $\Delta Z_o \approx -\frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * \frac{\Delta d}{d}$. Here d is small and because of that the via impedance is much more sensitive to it. For instance, 1mil change in via diameter d=8mil can cause about 4.3 Ohm change in the impedance (about 27.7dB in RL. Similar high sensitivity of via parameters to via diameter was observed in in [2]. This may be the major source of the via impedance discrepancies.

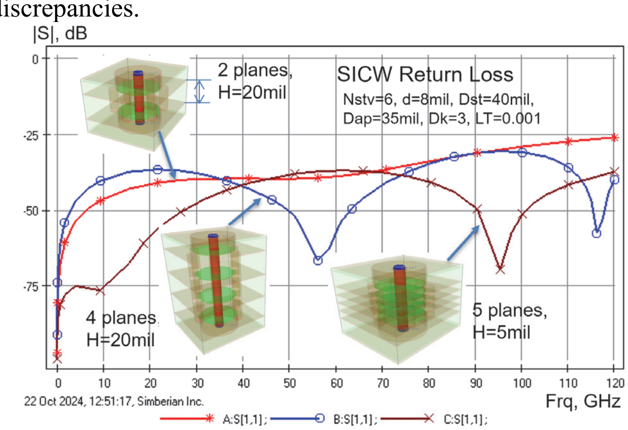

Fig. 2. Return loss for three SICW middle sections with same geometry in XY-plane and different stackup structure.

To validate SICW sensitivity to inter-plane distance and number of planes, we have simulated three SICW with different number of planes and distances between the planes (H) – the results are show in Fig. 2. De-embedded coaxial ports are used here at the top and bottom of vias. Simbeor 3DML solver is used for the analysis [11]. As we can see, the planes change the reflections from SICW, but the range of changes is acceptable to fit a large range of stackups and keep the reflection below -25dB.

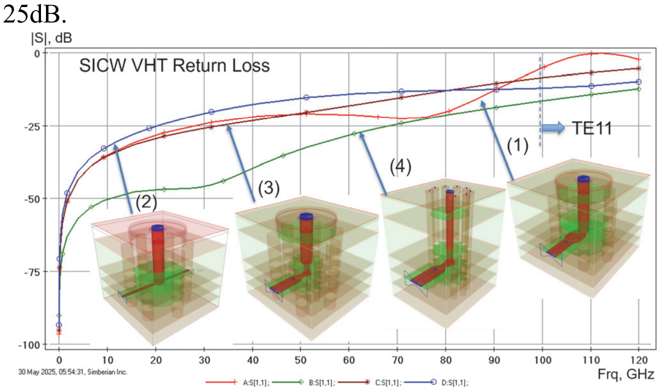

Fig. 3. Return loss for four possible VHTs.

Vertical to horizontal transitions (VHT) for SICW are actually transformers of quasi-TEM mode of the SICW to quasi-TEM mode of a strip or coplanar transmission line. Four possible configurations of VHTs from SICW to coplanar traces are shown in Fig. 3. Cases (1)-(3) are for the earlier discussed SICW suitable for 228 Gbps with the drill diameter 8 mil. Via (1) illustrates the “brick-wall” reflections caused by the quasi-TEM to quasi-TE11 mode transformation [7]. At about 110 GHz, TEM mode of coplanar trace is completely transformed into TE11 mode of the SICW. Depending on the boundary conditions for TE11 mode, it may cause complete reflection with short-circuit conditions as shown in Fig. 3, or complete transformation into TE11 port. Possible way to overcome the mode transformation is illustrated by case (2) – it is symmetric breakout into two 100-Ohm traces, that can be further merged back into 50-Ohm trace. Another option is to “tapper” the 8-mil via with a 4-mil micro via as illustrated by case (3). Though, this single mode transition is largely capacitive and may be susceptible to manufacturing variation as the structure (2). To ensure the single mode operation of via for 448 Gbps signals, smaller 4-mil vias with Dst=20mil has to be used and this is case (4) in Fig. 3.

IV. Substrate Integrated TwinAx Waveguide

The SIW design approach for single-ended vias can also be applied to differential vias. Twinax cable [10] serves as a prototype for constructing a substrate-integrated twinax waveguide (SITW) for the middle section of a differential via. The approach is similar to the conversion of coaxial into SICW - replacing the outer conductor with stitching vias sufficient to minimize leakage [7] and using large antipads with the effective size of the waveguiding structure to reduce misregistration sensitivity. Stitching vias are an essential component of the SITW structure.

The first step in SITW design is determining the stitching via placement for a given drill diameter and via spacing. An example of an SITW design that remains relatively independent of the number of planes and inter-plane distance is shown in Fig. 4. The target impedance is 85 Ohm, and we select an SITW configuration with approximately 87.5 Ohm impedance in the absence of planes. Closer planes may reduce impedance by a few Ohms. We conclude that SITW can serve as an any-stackup via. The critical design parameters for SIW are via diameter (d), signal via spacing (Dvv), and stitching via distance (Hstv). This example uses an oval pattern with eight stitching vias.

Regarding VHT, as with single-ended vias, it may be the most challenging aspect of differential via design. Fig. 5 presents two examples of transitions from SITW to differential traces. VHT (1) is the simplest straightforward connection and (2) is a transition with attempt to compensate the pad-to-pad capacitance by use of narrower traces over the antipads. Though, the vias remain capacitive mostly due to pad-to-pad capacitance and the high-order modes restrict the vias bandwidth to about 97 GHz.

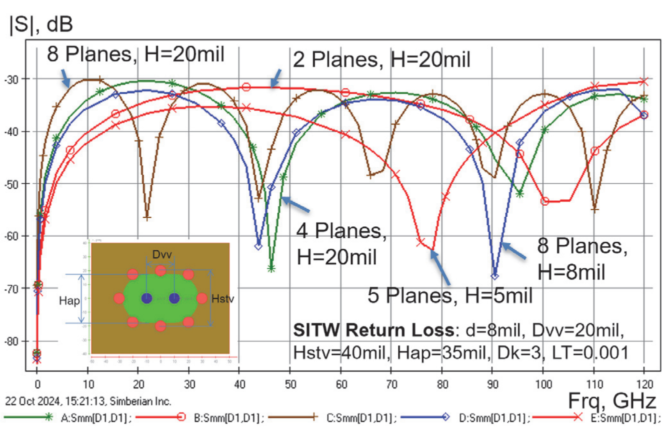

Fig. 4. Return losses for five SITW middle sections with same geometry in XY-plane and different stackup structure.

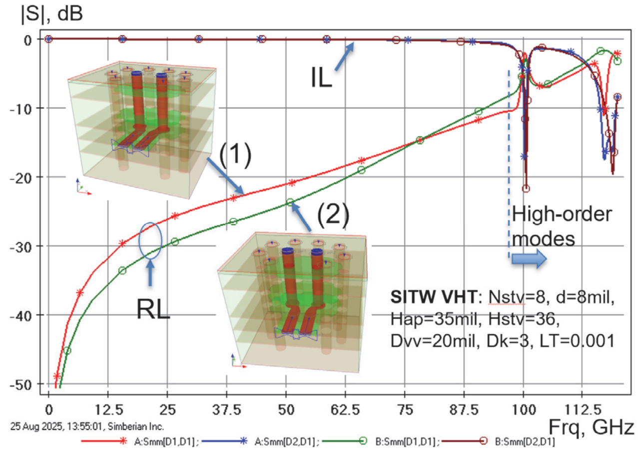

Fig. 5. Return losses (RL) and Insertion losses (IL) for two possible VHT from SITW to coplanar differential line.

V. Conclusion

This paper presents a novel waveguiding approach to designing any-stackup PCB and packaging vias for high-speed applications exceeding 120 GHz. By employing waveguiding structures -SICW and SITW - and segmenting vias into middle sections and transitions, we achieve a robust, manufacturing-tolerant design. Our numerical analysis confirms that SICW and SITW middle sections remain largely unaffected by stackup adjustments and variations and possible mis-registrations, making this methodology well-suited for bit rates up to 448 Gbps. While the approach is still a work in progress, we plan to test it further in practical scenarios.

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