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# Via Design for 112 Gbps and Beyond: Theory and Reality


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## Abstract

This work presents a novel approach of PCB vias design and optimization for 112 and 224 Gb applications. As data rates go up, vias are becoming increasingly important for signal integrity yet increasingly challenging in successful real-life implementation due to the necessity of tighter control over via's properties such as signal reflection, dissipation, and crosstalk at higher frequencies. Vias design is often becoming the limiting factor for the ultra-high-speed channel performance. To make matters worse vias electrical performance at high frequencies is often dominated by PCBs and Package manufacturing variations. We explore the physics of vias – conditions and metrics for localization within single-mode bandwidth up to 120 GHz. A novel approach is introduced to design for robustness against manufacturing variation, stackup adjustments due to copper density or multi-sourcing support. We demonstrate a practical design methodology prioritizing low sensitivity to these factors while meeting the low reflection criteria. The paper demonstrates some insights into the practical discrepancies between theoretical designs and manufactured vias, bridging the theory with realities.

## Authors Biography

**Alex Manukovsky** is a Technical Lead of the Hardware Engineering Technology team at Intel's Network and Edge Group (NEX), responsible for Signal and Power Integrity of NIC products. Alex focuses on MCP and SCP design for IPU (sNIC) and fNIC markets. He is leading the SI/PI activities, defining PCB and Package design guidelines for internal and external customers. His areas of expertise include simulation, modeling, and analysis of high-speed serial links for PCIe, Ethernet and DDR interfaces. His past work focused on channel and SerDes I/O modeling, robust de-embedding and calibration techniques. His experience includes developing test equipment as well as lab measurement methodologies for compliance testing of serial I/O's. Alex joined Intel in 2010 after receiving his BSc in Electrical Engineering from the Technion – Israel Institute of Technology. In 2019 he received his Master's degree in System Engineering from the Technion – Israel Institute of Technology.

**Yuriy Shlepnev** is President and Founder of Simberian Inc., where he develops Simbeor electromagnetic signal integrity software. He received a M.S. degree in radio engineering from Novosibirsk State Technical University in 1983, and a Ph.D. degree in computational electromagnetics from Siberian State University of Telecommunications and Informatics in 1990. He was the principal developer of electromagnetic simulator for Eagleware Corporation and a leading developer of electromagnetic software for the simulation of signal and power distribution networks at Mentor Graphics. The results of his research are published in multiple papers and conference proceedings.

**Joshua Nutzati** is an Algorithms Engineer at Intel's Network and Edge Group (NEX), responsible for building software tools for big data analysis, automation, simulation, and DSP. His work is focused on optimizing design flows, scaling existing capabilities, and integrating new software solutions for the Hardware Engineering Technology team. Joshua received his BSc in Aerospace Engineering from Embry-Riddle Aeronautical University in 2015.

**Alexander Kuntsevych** is a Senior Signal Integrity Engineer within Signal & Power Integrity team at Intel Networking Division, with over a decade of experience in high-speed board and package design , simulation of numerous serial and parallel high speed interfaces. Currently with Intel specializes in signal integrity analysis and optimizations of pcb and package performance, interconnect quality analysis and compliance for advanced pcbs and multidie packages. Alexander joined Intel in 2021 after 7 years at WDC as Senior SI/PI Engineer. He holds a BSc in Electrical Engineering from the Technology University of Dahl in Ukraine

**Itzhak Peleg** has been engaged in signal integrity since its inception. Encountering it as early as a Technion student, shortly before the turn of the millennium. Solved and developed flows in order to face the ever-increasing challenges on the way. He has worked for the leading companies Marvell, Western Digital, and now Intel. Specialized in the simulation of large systems like DDR. Extraction of models with leading tools: HFSS, PowerSi, Simbeor. Working on ETH, PCIe, UFS, and more. Experience 20y+ in package and board design for SI.

**Shimon Mordooch** is a SIPI team Lead at NEX Intel. He has over 28 years of experience in various hardware design aspects in telecommunications and networks, covering design and managerial positions.
Through the years he was involved in chassis designs starting as a board designer all the way to the system level definitions of the whole chassis, its backplane, signal/power integrity, and management. In recent years he is working in the cable edge industry and more focused on the hardware technological aspects, starting from in-depth
characterization and selection of building blocks (for example, PCB materials, highly dense system design, etc.) through detailed SI/PI simulation analysis and at the end - full lab characterization of all hardware aspects of the system.

# Introduction

Designing PCB and packaging interconnects for 112-224 Gbps presents multiple challenges, with the design of vertical transitions, or vias, being one of the most critical. Vias can dissipate and reflect signals, contributing to crosstalk noise through both local and distant coupling to other links. The primary goal of via design is to reduce reflection over the signal bandwidth or as observed on Time Domain Reflectometry (TDR). This paper introduces additional goals: increasing single-mode bandwidth and localization, and reducing sensitivity to manufacturing stackup adjustments and geometry variations. We propose a new methodology for via design that minimizes sensitivity to stackup adjustments while meeting localization and reflection goals, providing insights into the practical discrepancies between theoretical designs and manufactured vias.

Compared to traces or transmission lines, vias are more complex structures and often major contributors to signal degradation. Reflections and dissipation by vias increase overall signal losses. Reflections and crosstalk appear at the receiver as uncorrelated bounded noise, reducing the channel operating margin and resisting mitigation by equalization techniques. Reducing reflections over the signal bandwidth is a common goal in via design. Another goal is to minimize crosstalk by increasing via localization, allowing for simulation in isolation from the rest of the PCB. This paper introduces a formal approach to evaluate localization using 3D electromagnetic (EM) modeling in isolation with infinite-plane boundary conditions and comparative analysis of dissipated powers.

Additional challenges in via design arise from manufacturing considerations. PCBs are not always manufactured as designed. When a PCB design is sent to different manufacturers, they adjust it based on available laminates and supported manufacturing capabilities for each. Consequently, PCBs produced by different manufacturers often have varying materials and stackup dimensions. Part of the impedance-controlled manufacturing process involves adjusting trace widths to meet impedance goals. Though, vias geometry remains the same and ideally designed low-reflection vias may exhibit unacceptable reflections with a modified stackup, which can only be revealed at the post-layout stage when manufacturing adjustments are known. This may be too late in the design cycle, introducing additional uncertainties and reducing overall margins. Redesigning each via for each manufacturer complicates the process and is undesirable. To address this, we introduce two new approaches for designing vias that are less sensitive to anticipated stackup adjustments and to manufacturing variations.

The paper is structured as follows. First, we provide an overview of the recent advances in via analysis and design. Next, we investigate via localization and introduce dissipated power as a metric for evaluation of possible leaks and coupling. Then, we introduce a new simultaneous optimization approach to design vias for two similar stackups. This approach is tested with reality in the next chapter and found to be sensitive to manufacturing variations. In the final chapter, we propose a more robust, any-stackup approach based on designing vias as substrate-integrated waveguiding structures. This new method has yet to be verified in practice.

## State of the Art in Via Analysis and Design

The extensive use of vias through multiple layers is a distinctive feature of digital interconnects. Via modeling and design techniques have primarily been developed for digital interconnects and continue to evolve as data rates increase.

For data rates below 1 Gbps, single LC models are typically sufficient [1,2]. For data rates up to 6 Gbps, distributed ladder-type LC models may be adequate [2]. At these frequencies, PCBs or packages are electrically small, and vias generally act as minor capacitive or inductive discontinuities that do not significantly affect the signal. The primary design requirement at these data rates is the connectivity of the reference conductors. To enhance accuracy, L and C values can be calculated using static and magneto-static solvers or infinite radial waveguide or parallel-plane models. Note that such models are applicable for well localized vias within single-mode bandwidth.

As data rates exceed 6 Gbps, additional challenges arise due to via coupling with large parallel-plane power delivery networks (PDNs). These challenges can be addressed in two ways: using via models that include 2D electromagnetic models of parallel planes [3-15] (the hard way) or localizing vias with a sufficient number of reference or stitching vias [17] (the easy way). Via coupling with PDNs complicates the analysis of digital interconnects, involving electrically oversized planes spanning the entire board. This analysis can only be performed using simplified 2D EM methods. An overview of earlier works on this subject can be found in [6], and recent progress is surveyed in [13-15]. Initially, via coupling models were based on “intuitive” physics-based approaches accurate for structures with small inter-plane distances [3-11]. Later works [12-15] are based on the original work of Williamson for the antenna applications [16]. The improved physics-based approach includes high-order modes near vias and mode transformation between vias and 2D PDN models, extending via model accuracy up to 100 GHz [14-15]. However, this accuracy is valid for relatively simple via geometries and does not eliminate need for accurate 3D EM modeling. For practical cases, the accuracy of reflection and insertion loss evaluation may be insufficient even at lower frequencies. Despite this, via analysis with PDNs remains the only viable solution for analyzing long-range or distant coupling/crosstalk between vias, provided they are not sufficiently localized. Via models that include parallel planes are available in several commercial signal integrity solvers. These tools can evaluate coupling between poorly localized vias in the context of 112 Gbps interconnect analysis, though such analysis is complex and can be avoided by increasing via localization [17]. This paper provides a formal methodology for evaluating extending via localization and bandwidth.

For data rates above 6 Gbps, via analysis and optimization are dominated by 3D full-wave electromagnetic analysis [18-22]. This analysis is typically applied to a small area around single-ended or differential vias with stitching vias to evaluate reflection and transmission. It may also include multiple signal vias to evaluate local coupling between them and possibly traces. The analysis can be performed using finite integration technique (FIT in CST) [6], finite element method (FEM in HFSS or Clarity) [18, 20-21, 23], boundary element method (BEM in HyperLynx 3DEM) [19,22], or method of lines (MoL in Simbeor 3DML) [17]. However, 3D EM analysis does not guarantee via model accuracy, which depends on boundary conditions and port formulation. Most importantly, it depends on via localization. The behavior of unlocalized or poorly localized vias is unpredictable when simulated in isolation with any type of 3D EM analysis. This will be

elaborated on and illustrated with numerical experiments in the next chapter. Recent advancements in whole-package analysis with FEM accelerated by domain decomposition [23] and BEM [22] are impressive, but the accuracy proof for such large-scale problems is unconvincing, and analysis times are too long. Also, PCBs are usually more complex compared to the package benchmark example. As in the case of 2D EM analysis, better localization is the alternative. **Increasing localization withing the single-mode via bandwidth should be a design goal, as demonstrated in this paper.** The recent advancements in via manufacturing allow design of vias localized up to 120 GHz and beyond.

Finally, emerging hybrid 2D+3D analysis techniques combine the accuracy of 3D EM analysis with the capabilities of 2D EM models to account for distant coupling [24-26]. These techniques are promising for those who decide to neglect the localization, but they are still in the research stage, and their necessity will depend on the importance of long-range coupling. Again, it is either hybrid analysis (difficult) or increase of localization (easy).

Regarding via design techniques, the mainstream approach is direct optimization with 3D EM solvers [18-21]. However, indiscriminate optimization of all via parameters may lead to complex structures sensitive to manufacturing variations and with too many parameters increasing computational effort and design resources. Understanding and application of via physics is important, to avoid the overdesign. Simultaneous direct optimization of vias to different layers simplifies design and allows the use of the same padstack for different layers [19]. We use a similar approach of simultaneous optimization to use the same padstack for two different stackups. Though, it turned out that the final structures were too sensitive to the manufacturing variations. Additional design simplification is possible with the domain decomposition [27] or “zones” approach [28]. A via is divided into a middle section and vertical-to-vertical (transition to an SMA connector) and vertical-to-horizontal transition (via to trace). This paper uses this approach as an alternative to the simultaneous optimization. The design of the middle section is further simplified by turning it into a segment of a substrate-integrated waveguiding structure with small discontinuities and very low sensitivity to antipad misregistration and dielectric constant variations.

# Analysis Bandwidth and Localization

The most important property of vias is localization, which defines the predictability of all other via parameters (reflection and transmission) and the overall accuracy of interconnect analysis. **A predictable via should be localized over a substantial part of the signal spectrum.** In this chapter, we will introduce a formal metric for localization.

First, let's define required bandwidth for different types of via analyses. Bandwidth can be formally defined by the signal source spectrum, taking into account the expected signal degradation in the package and link. Signal degradation reduces the power in high-frequency harmonics, thereby reducing the bandwidth required for analysis. Power spectral density (PSD) can be used to evaluate the bandwidth, as illustrated in Fig. 1 for a 112 Gbps PAM4 signal with a 4ps rise time. Fig. 1 shows the PSD of the original signal and the PSD for the same signal transmitted through a 10-inch trace.

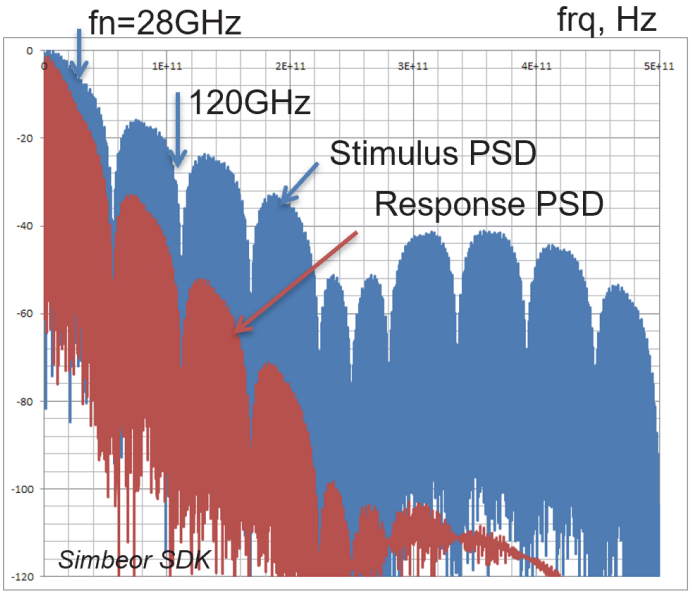



Fig. 1. PSD for 112Gbps PAM4 signal, 4ps rise time – blue plot; PSD transmitted through 10-inch strip line: W=12mil, H=20mil, Meg7 – Wideband Debye: Dk=3.17, LT=0.0011 @ 1 GHz, Copper: RR=1.4, Roughness – Huray- Bracken Model: SR=0.14 um, RF=8.7.

As we can see, the analysis of insertion loss (IL) and far-end crosstalk (FEXT) may require smaller bandwidth due to the attenuation of high-frequency harmonics. Only 1.5-2 Nyquist frequencies (fn=28GHz in this case) may be sufficient for accurate analysis of the transmitted signal. More accurate formal pulse analysis can be used for a better estimate [29]. However, the spectrum of near-end crosstalk (NEXT) may be practically the same as the stimulus if aggressor vias and traces are close to a victim link. The maximum possible bandwidth should be used for NEXT analysis. We will use a 120GHz bandwidth for localization and crosstalk investigation, which is 3x Nyquist frequencies plus an extension to illustrate the effects of via breakout.

$$\boldsymbol{P_{out} = P_{in} - P_{reflected} - P_{dissipated} - P_{leaked} + P_{coupled}}$$

$$P_{in} = |a_1|^2\ [Wt], a_2 = 0$$

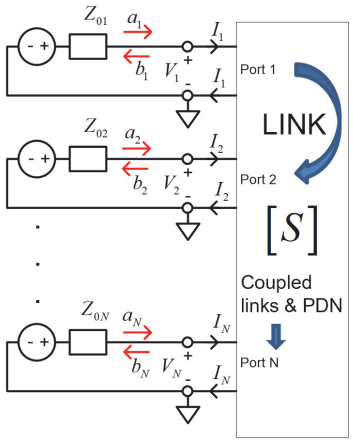
$$P_{out} = |S_{2,1}|^2\ P_{in}$$

$$P_{reflected} = |S_{1,1}|^2\ P_{in}$$

$$P_{dissipated} = \left(1 - \Sigma_k |S_{k,1}|^2\right) P_{in}$$

$$P_{leaked} = \left(\Sigma_{k\neq 1,2} |S_{k,1}|^2\right) P_{in}$$

$$P_{coupled} = \left(\Sigma_{k\neq 1,2} |S_{2,k}|^2\right) P_{ink}$$




$$\tilde{a} = \frac{1}{2} Z_0^{-1/2} \cdot (\tilde{V} + Z_0 \cdot \tilde{I})$$

$$\tilde{b} = \frac{1}{2} Z_0^{-1/2} \cdot (\tilde{V} - Z_0 \cdot \tilde{I})$$

$$\tilde{a}, \tilde{b} \in C^{N\times 1}$$
$$Z_0 = diag\{Z_{0i}\} \in R^{N\times N}$$

Scattering parameters:
$\tilde{b} = S \cdot \tilde{a} \quad S \in C^{N\times N}$

$$S_{i,j} = \left.\frac{b_i}{a_j}\right|_{a_k=0 k\neq j}$$

Fig. 2. Balance of power and definition of elements through S-parameters for a link coupled to other links and PDN.

The energy difference between the Power Spectral Densities (PSDs) of the stimulus and response in Fig. 1 can be explained by the balance of power shown in Fig. 2 with all elements defined through S-parameters [30]. The balance is valid in time-domain and in frequency-domain over the bandwidth of the signal. It is assumed that a driver is at port 1 and a receiver at port 2 and S-parameter model includes coupling with some other links and, possibly, with the power distribution networks (PDN). $\boldsymbol{P_{out}}$ is the power of signal at a receiver. The power from a driver $\boldsymbol{P_{in}}$ is absorbed in dielectrics, conductors and boundaries ($\boldsymbol{P_{dissipated}}$), reflected back to the driver ($\boldsymbol{P_{reflected}}$) and, possibly, leaked ($\boldsymbol{P_{leaked}}$) to coupled structures. The last term in the balance of power $\boldsymbol{P_{coupled}}$ is the power gained from the coupled structures (other links and PDNs). As we can see, it is defined with S-parameters reciprocal to the leaked power, assuming that the excitation is at the port 2. $\boldsymbol{P_{leaked}}$ is a type of loss that includes leaks to other signal links through local coupling and leaks through PDNs to other links (distant coupling). The later happens at the un-localized or leaky vias. It is relatively easy to simulate the local leaks and coupling – it can be done with the analysis of a few links or vias in isolation from the rest of the board. However, the analysis of the distant leaks and coupling may require analysis of the whole board with PDNs. That is not desirable. Can we evaluate possible distant coupling with an analysis of a link or via in isolation? The analysis in isolation means that $\boldsymbol{P_{leaked}} = 0$ and $\boldsymbol{P_{coupled}} = 0$. If we do such analysis with an absorbing boundary condition (ABC) the dissipated power can be expressed as follows:

$$\boldsymbol{P_{dissipated}} = \boldsymbol{P_{absMat}} + \boldsymbol{P_{absBC}}$$

Here $\boldsymbol{P_{absMat}}$ is power absorbed by materials (dielectrics and conductors) included in the model and $\boldsymbol{P_{absBC}}$ is the power absorbed by the boundary conditions. Let's investigate if $\boldsymbol{P_{absBC}}$ can be used as a measure of possible via leaks and distant coupling. The energy leaving the structure through the boundaries should give us a measure of possible absorption by the rest of the board and leaks or coupling in actual board.

But first, **what boundary conditions (BC) to use and how to evaluate the energy absorbed by it?** Considering the BC, we choose perfectly matched layer (PML) conditions that imitate the infinite planes. This should be considered as the worst-case scenario – the impedance of actual planes is lower than the infinite planes due to stitching and decoupling structures. The infinite-plane BC are implemented in Simbeor 3DTF solver based on Trefftz finite elements. Considering the escaped energy value, ideally, we have to compute the power absorbed by boundaries directly. Though, it requires computation of fields at the boundary, that is not convenient. An alternative is to use comparative analysis of the insertion loss [31] or power losses [32]. We will compute and compare $\boldsymbol{P_{dissipated}}$ for structures with different localization. Another way is to do the analysis of the same structure without losses in materials – only with the lossy boundaries [33]. Thought, the removal of the losses changes the physics of the problem.

To investigate possibility of simulation of distant coupling in isolation and the effect of via localization with stitching vias, let's simulate and compare two very simple structures shown in Fig. 3. Two 0.77mil copper planes, separated by dielectric with Dk=3, LT=0.001. Two single-ended signal vias with 10mil diameter are separated by about 220mil. Stitching vias connect both planes and are located at 20mil from the signal vias. As was shown in [14], the reduced model with single cavity or with infinite planes is sufficient to predict crosstalk in via arrays. This numerical example is the worst-case

scenario – in reality the planes usually have more stitching vias that suppress the resonances at lower frequencies and reduces the impedance.

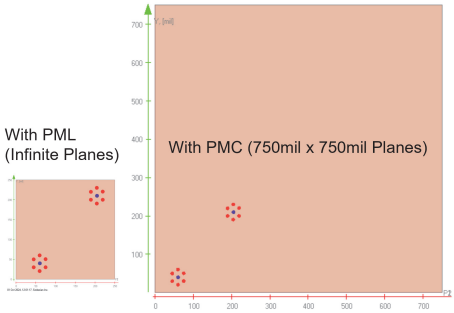



Fig. 3. Two problems to investigate the localization effect on distant coupling – large square problem with PMC conditions (right) and small cut-out with PML boundary conditions (left).

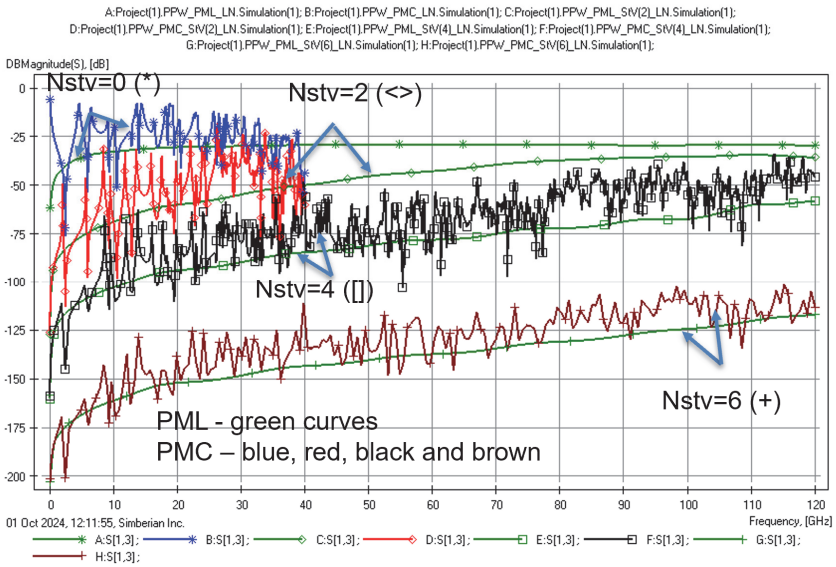



Fig. 4. Magnitudes of coupling between two vias between two parallel planes separated by 9mil with different number of stitching vias and PMC (blue, red, black and brown) or PML (green) boundary conditions.

Magnitudes of coupling between the vias computed with different number of stitching vias (Nstv) are shown in Fig. 4. “Intuitive” physics-based model [5] with 2D analysis in Simbeor 3DTF solver is use for the analysis. As we can see, the increase of stitching vias reduces the coupling. The dramatic increase in the isolation with the number of stitching vias greater than 2 was also observed with sensitivity analysis in [34]. As we can also see from the plots, the coupling saturates with the frequency – that remarkable phenomenon was also observed in [12, 14]. Fig. 4 shows results for distance between planes 9mil. The coupling decreases with the decrease of the inter-plane distance and increases as the distance becomes larger. As we can observe, the coupling between the vias with finite planes has a lot of resonances – even with relatively small planes as in this example. Complexity of a problem with the actual geometry of the planes may be enormous – for instance, accurate analysis of very simple problem resolving all those resonances up to 100GHz may take over 10 hours with an advanced 3D FEM solver [15]. Can we evaluate the vias with the infinite plane model and what we lose in this case?

That option was also investigated in [10]. From the example shown in Fig. 4 we can see that the coupling estimated with infinite planes (green curves) is not accurate with the small number of stitching vias. However, the estimate is becoming better with the increase of Nstv. This investigation is done for one plane pair. Power sum crosstalk (PSXT) is growing approximately as the square root of the number of distant aggressors *Naggr* or as $\Delta_{PSXT} \approx 10 * log10(Nagr)$ and it is not very sensitive to the distance between the victim and aggressors [34]. That simple and easy experiment can provide a guidance on the expected distant crosstalk.

Dependences the insertion loss (IL) and reflection loss (RL) from the localization are shown in Fig. 5. As we can see, the model with infinite planes becomes more accurate as the number of stitching vias grow. That effect was also observed by multiple authors, for instance in [7, 10, 31]. The reflections on Fig. 5 are relatively high in this example, because of only the plane pair impedance is included in the model (no via-to-plane capacitance).

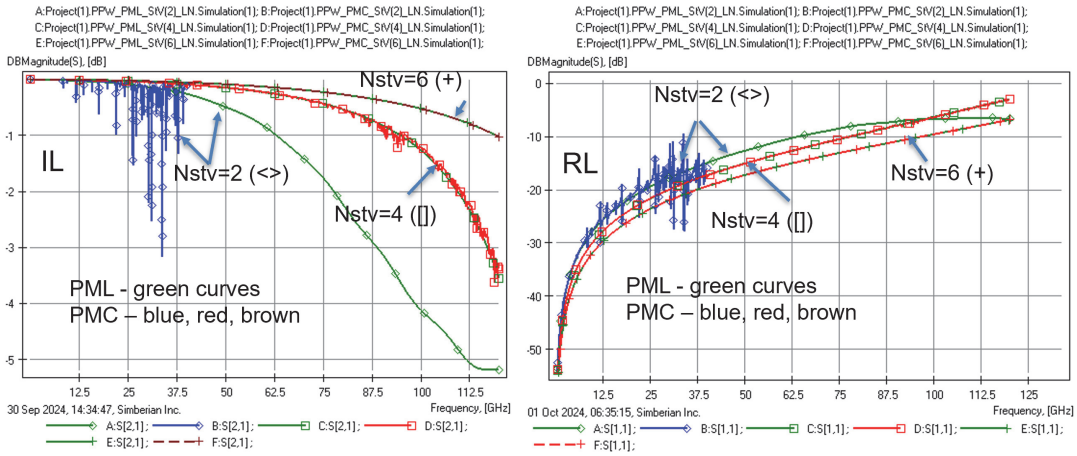



Fig. 5. Magnitudes of IL (left plots) and RL (right plots) for a signal via between two parallel planes with different number of stitching vias (Nstv) and PMC (blue, red, and brown) or PML (green) BC.

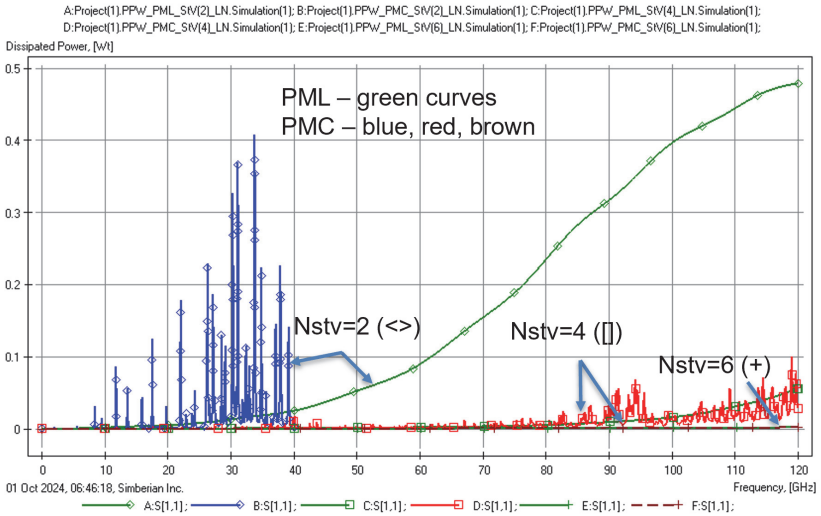



Fig. 6. Dissipated power for a signal via between two parallel planes with different number of stitching vias (Nstv) and PMC (blue, red, and brown) and PML (green) BC computed with 2D EM model.

Finally, comparison of the power dissipated by a via in infinite and finite planes is shown in Fig. 6. Dissipated Power (DP) is computed for 1 Watt excitation. Notice that the DP computed with the finite and infinite planes exhibit behavior similar to the IL and RL results. We can see that with 6 stitching vias analysis in isolation gives IL, RL and DP practically the same as with the finite planes. On the other end, use of just 2 stitching vias is clearly insufficient for the accurate analysis in isolation or with the infinite planes – such vias are under high influence of the PDN structures (resonances in Fig. 5 and 6).

So far, we have a few important observations from the simple numerical experiment with the physics-based 2D electromagnetic model of vias:

- **Stitching vias reduce coupling and suppress effect of resonances in PDN;**
- **Stitching vias reduce dependency of RL/IL on PDN geometry;**
- **Infinite planes or PML BC can be used to evaluate possible coupling;**
- **Stitching vias reduce dissipated power;**

To confirm it with 3D EM analysis that includes high-order modes around via and to demonstrate that the **dissipated power can be used as the measure of via isolation** for estimate of possible leaks and coupling, a single via with different number of stitching vias is simulated with Simbeor 3DTF solver with the **special PML boundary conditions with plane continuation**.

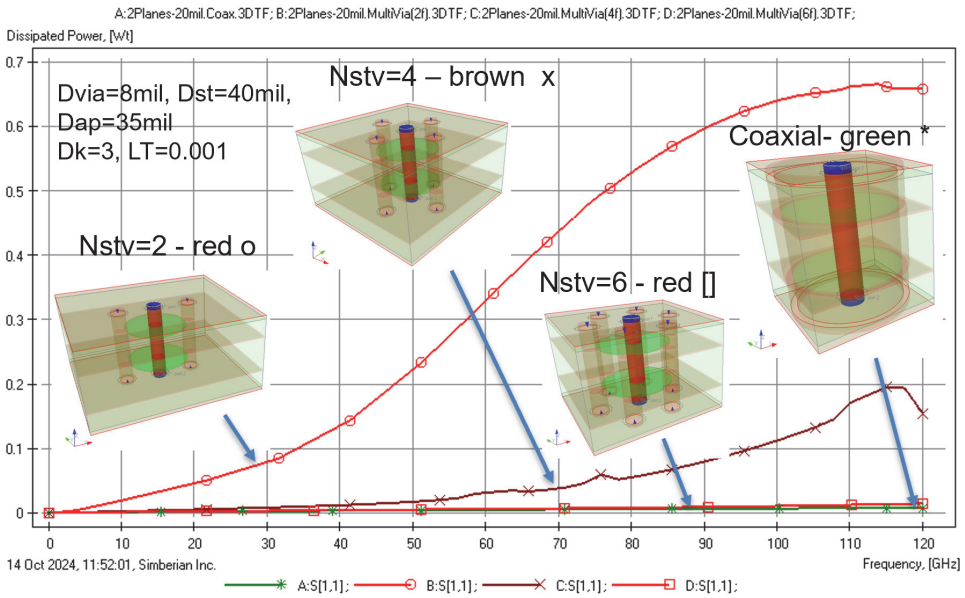



Fig. 7. Comparison of dissipated power for a via between two parallel planes with different number of stitching vias (Nstv) and PML boundary conditions and with coaxial via (3D EM model).

Comparison of the power dissipated by a single via with different number of stitching vias is shown in Fig. 7. The vias are crossing 2 parallel planes separated by 20mil. Deembedded multiconductor transmission line ports are located at the top and bottom planes of the structures. Minimal possible dissipated power is evaluated with an ideal coaxial via (green curve with stars). This analysis includes the high-order modes in the vicinity of vias and propagating modes behave as in infinite planes. Similar to 2D analysis, 3D models shows that the DP for a single via with just 2 stitching vias is

considerably higher than in the case with 6 and even 4 stitching vias. On the other hand, DP of a via with 6 stitching vias (red line with squares) is very close to power dissipated by the ideal coaxial segment without any leaks (green line with stars). Fig. 8 illustrates the process of signal propagation in the via with 2 stitching vias (3 top pictures) and in the via with 6 stitching vias (3 bottom pictures) with power flow density (PFD) computed at 10, 50 and 100 GHz. Arrows size and color correspond to PFD expressed in dB. As we can see, the via with 2 stitching vias visibly leaks energy even at 10 GHz and the via with 6 stitching vias has very small PFD directed toward the boundaries even at 100 GHz. Values of the DPs in % of the input power are also shown in the Fig. 8.

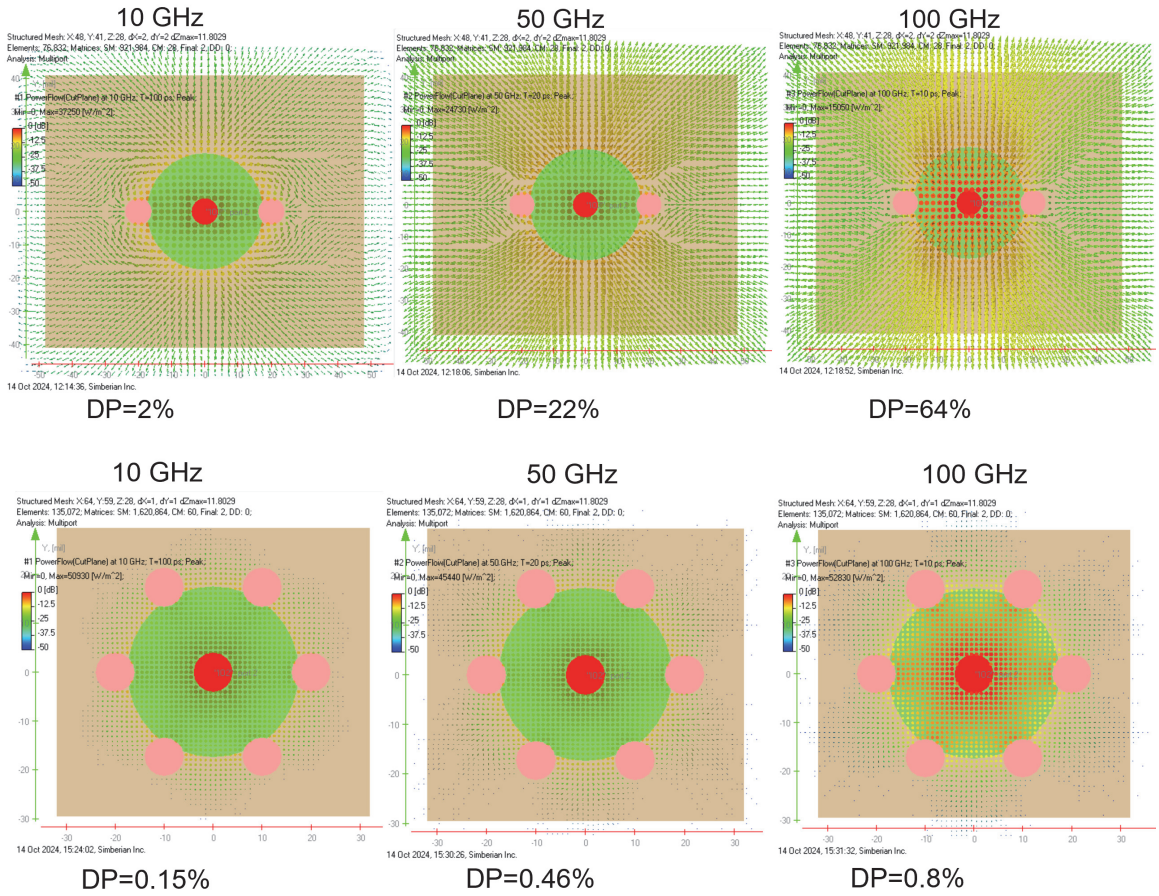



Fig. 8. Peak power flow density in single-ended via with 2 (top) and 6 (bottom) stitching vias.

Fig. 9 illustrate the dependency of DP on the number of parallel planes and distance between the plane. As we can see, the leaks grow with the number of plane pairs NL approximately linearly $\Delta_S \approx \mathbf{20} * \boldsymbol{log}\mathbf{10}(\boldsymbol{NL})$. Also, DP growth rate increases at frequencies above about 90 GHz – this frequency is the bandwidth of the via.

To verify the correlation between possible coupling and the maximal DP, two single-ended vias with 6 stitching vias each and different distance between the signal vias were simulated. The coupling parameters are plotted in Fig. 10. Deembedded coaxial ports are used in this example. As we can see, the case with the closest vias has maximal coupling, but it does not exceed -50dB.

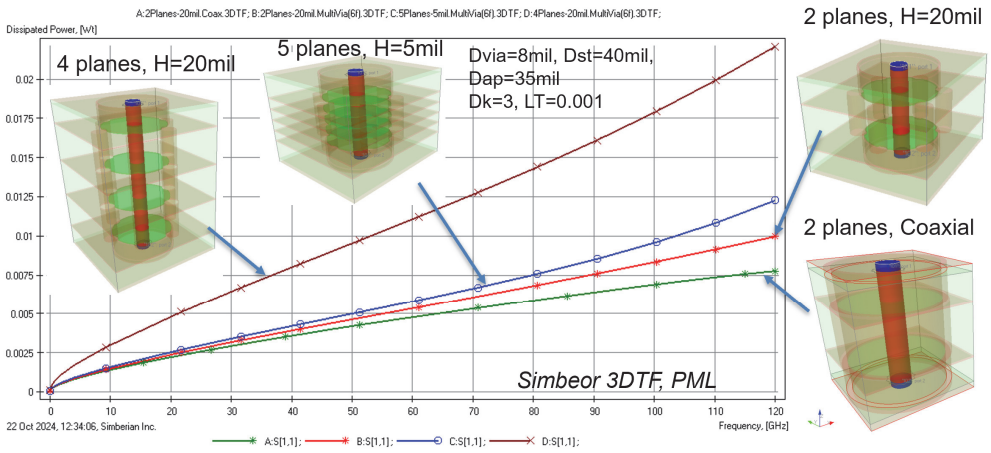



Fig. 9. Dissipated power for SE via with 6 stitching vias and different number of parallel planes. DP increase approximately proportional to the number of planes with the same distance.

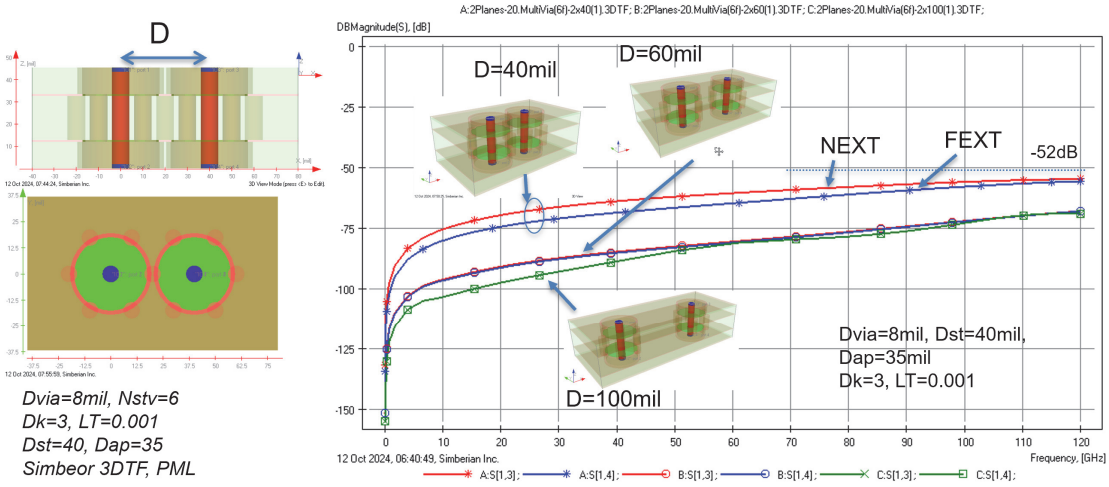



Fig. 10. Dependence of coupling between two single-ended vias with Nstv=6 from distance between vias (D) with 2 planes separated by 20mil, de-embedded coaxial ports.

**To improve the isolation, either more stitching vias on same circle or another circle of stitching vias can be used.** Note that isolation of larger areas that includes multiple vias with via fences may increase the coupling at resonances – it should be avoided or complimented with the local stitching.

Comparing to single-ended vias, differential vias have better localization as illustrated by DP in Fig. 11. DPs of differential mode for 3 structures with 2, 4 and 8 stitching vias are computed for comparative analysis of possible leaks and distant coupling. As we can see, only 2 stitching vias placed along the vias axis may be sufficient for the differential mode localization up to 20-30 GHz. More stitching vias is required to localize the differential mode up to 100 GHz and to localize common mode.

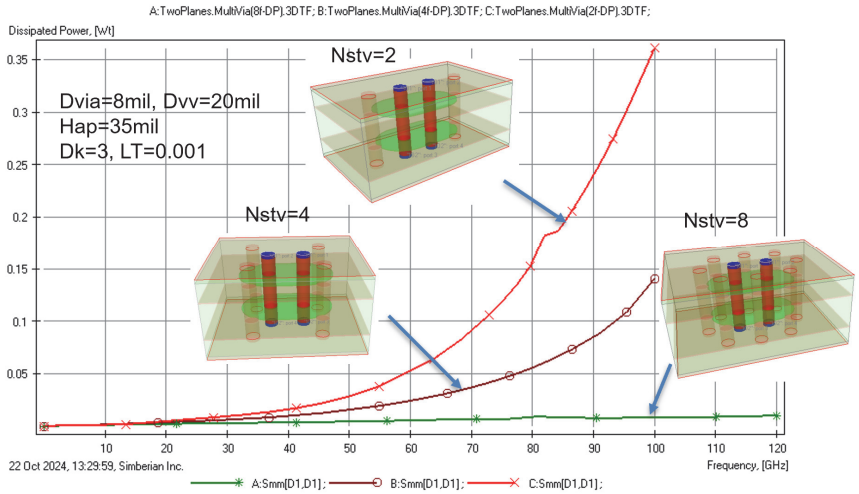



Fig. 11. Power dissipated by differential vias with different number of stitching vias (Nstv).

From these numerical experiments, we can conclude that evaluating possible via leaks and coupling can be effectively done through simulations in isolation using infinite plane boundary conditions and evaluating dissipated power. The actual limit on DP must be defined on a case-by-case basis. **The key takeaway from this investigation is that sufficiently localized vias can be simulated in isolation.** This can be done with any boundary conditions. However, if the analysis bandwidth exceeds the localization bandwidth (which is usually the case), absorbing boundary conditions (ABC) may be preferable. ABCs dampen numerical box resonances and reduce simulation time. These boundary conditions should have low impedance to mimic the behavior of large parallel planes with extensive decoupling and stitching. Capacitive ABCs were implemented in the Simbeor 3DML solver specifically for analyzing vias above the localization frequency. **In reality, resonances in PDN above the localization frequency define the via behavior and this is not predictable with any analysis in isolation.**

# Simultaneous Optimization Approach

In this chapter we design vias that should work in two similar stackups shown in Fig. 12 representing a single design manufactured by two different vendors . Here are the initial vias design goals:

- Ensure **localization** and bandwidth up to 2x Nyquist frequency (56 GHz)
- Make sure that the **reflections are below a target** defined by a polyline
- Use **one via design for two similar stackups**

To reach those goals, a solution space with possible vias geometries satisfying the localization and reflection criteria is built for two stackups. Next, each configuration is ranked by the distance from the reflection target – **the lower the reflection over the bandwidth of the signal, the higher the score**. Finally, the via with the highest score for two stackup modifications is selected for the production. Alternatively, the co-optimization approach introduced to design vias with identical padstack for different layers can be used [19].

To satisfy the localization requirement, 7 stitching vias are placed on circles with diameters ranging from 56 to 64 mil – the vias are localized up to about 100 GHz.

However, via bandwidth is defined by the TE11 mode cutoff frequency in this case as explained in the final chapter. The via bandwidth is only about 62 GHz for 64 mil stitching circle and 70 GHz for 56 mil. We consider that acceptable.

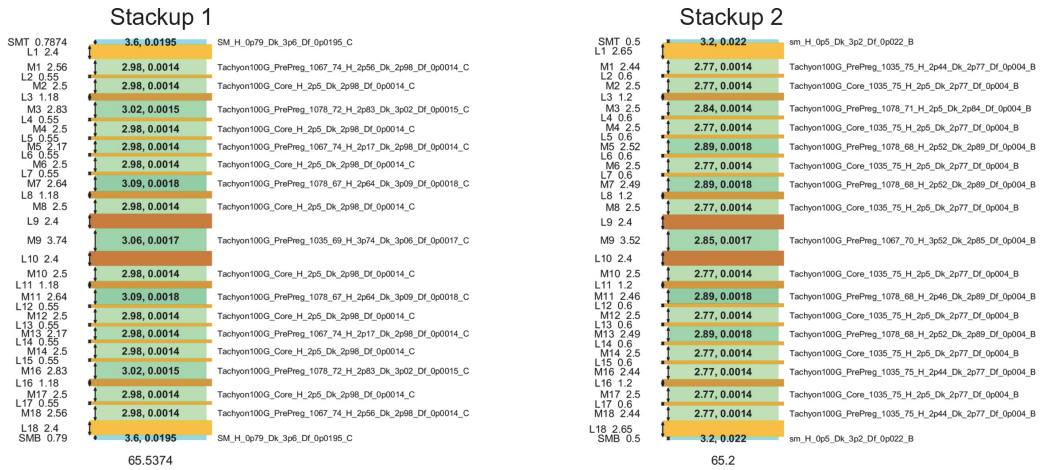
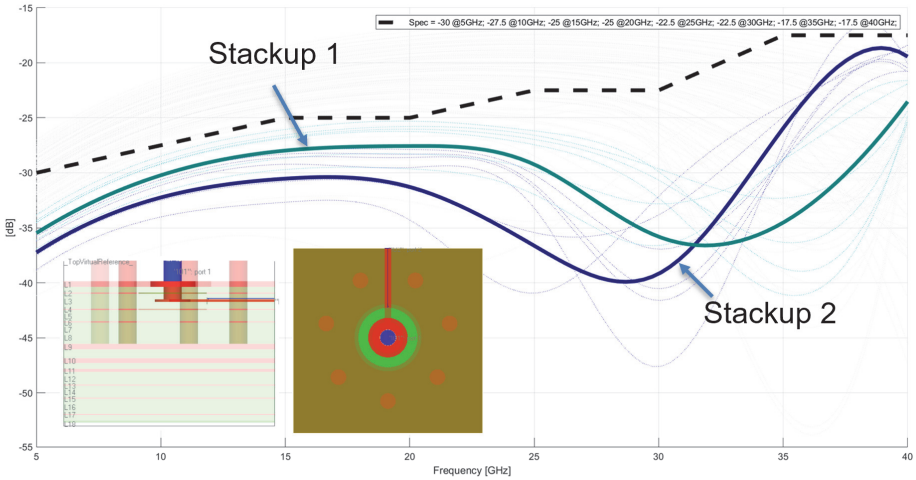


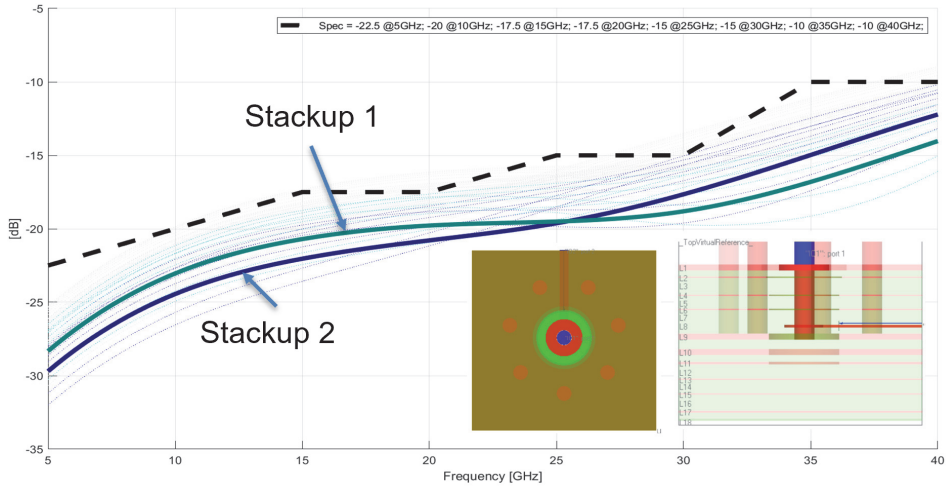

Fig. 12. Two stackups with similar materials from two vendors for a single via design.

Examples of the solution spaces and best configurations with highest scores are provided in Fig. 13-15. Some dimensions of vias are also shown in the tables in mils. Here Dap are antipad diameters at a particular layer. The other dimensions are self-explanatory. As we can see, the same geometry of vias can be successfully used for the board manufacturing by two different vendors. This is in theory so far. Let's do the reality check.



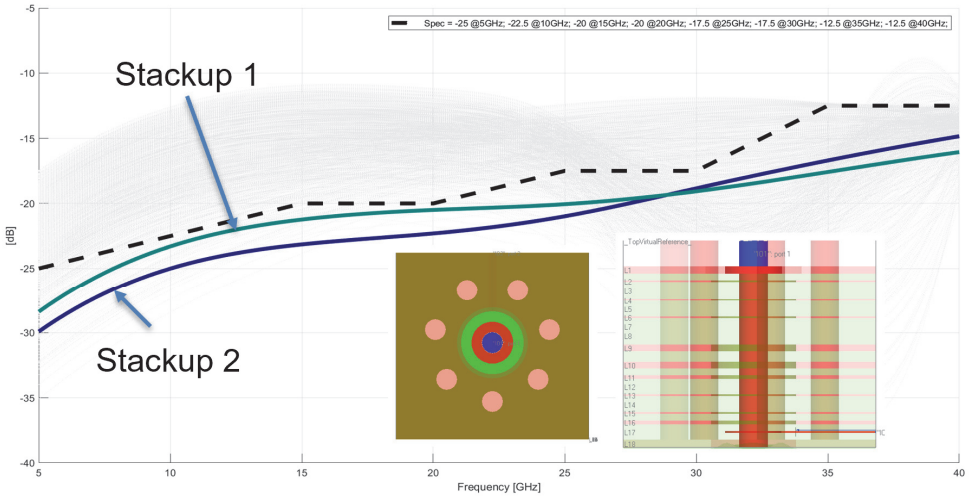

| Stitching Via Sep | Dap | Nstv | L1 Dap | L2 Dap | L4 Dap | Stackup 1 Score | Stackup 2 Score | Combined Score |
|---|---|---|---|---|---|---|---|---|
| 64 | 26 | 7 | 34 | 30 | 30 | 2.429509893 | 2.03653299 | 0.31468673 |
| 64 | 26 | 7 | 36 | 32 | 26 | 1.64567054 | 2.717909333 | 0.309837936 |
| 64 | 26 | 7 | 34 | 30 | 28 | 0.746389116 | 3.987584796 | 0.307893391 |
| 64 | 26 | 7 | 34 | 30 | 32 | 2.656124073 | 0.718457578 | 0.241546998 |

Fig. 13. Example of solution space for via to layer L3 and the best geometries with corresponding scores in 2 stackups. Reflections from the top-rated via in two stackups are shown by thick lines.




| Stitching Via Sep | Dap | Nstv | L1 Dap | L2 Dap | L9-L11 Dap | Sackup 1 Score | Stackup 2 Score | Combined Score |
|---|---|---|---|---|---|---|---|---|
| 64 | 28 | 7 | 34 | 30 | 28 | 1.552131892 | 1.58837021 | 0.234384737 |
| 64 | 30 | 7 | 34 | 30 | 30 | 1.510996014 | 0.574953612 | 0.192068919 |
| 64 | 28 | 7 | 36 | 32 | 28 | 0.814770212 | 0.85220771 | 0.176486944 |
| 64 | 26 | 7 | 34 | 30 | 26 | 0.231073771 | 1.413085464 | 0.157979642 |

Fig. 14. Example of solution space for via to layer L8 and the best geometries with corresponding scores in 2 stackups. Reflections from the top-rated via in two stackups are shown by thick lines.




| Via Drill | St. Via Drill | Stitching Via Sep | Dap | Nstv | L1 Dap | L18 Dap | Stackup 1 Score | Stackup 2 Score | Combined Score |
|---|---|---|---|---|---|---|---|---|---|
| 10 | 10 | 56 | 30 | 7 | 34 | 30 | 0.73156839 | 0.142555438 | 0.112078934 |

Fig. 15. Example of solution space for via to layer L17 and the best geometry with corresponding scores in 2 stackups. Reflections of the top-rated via in two stackups are shown by thick lines.

# Reality Check

Small batches of PCBs with the designed vias were manufactured by three different vendors, in order to evaluate the effect of manufacturing multistring of a single design. The results are summarized in Table 1.

The post manufacturing reality differs from intended design. First, we have observed large variations in the via impedances observed on TDRs as demonstrated in Fig. 16-18. TDR plots shown the target impedance value and lines for ±10% and ±15%

deviations. Next all boards were cross-sectioned and all critical dimensions were measured. As we can see, significant misregistration of antipads, vias and pads could be observed on several via structures. The data indicates some of the designed vias are more challenging to manufacture as designed then others. However, the challenge is not uniform across the tree vendors, and some of the deviation from design observed for some but not all of the vendors. The maximal values of misregistration are reported in Table 1.

Most of the issues identified here stem from changing stackup selected. While more common stackups and more advanced manufacturing techniques can yield better results. **The key takeaway from this investigation is that reliable vias should be designed with the additional goal of low sensitivity to manufacturing variations.** A potential solution is discussed in the next chapter.

Table 1. Summary of the problems observed on PCBs manufactured by 3 vendors.

| vendor | Tline structure | | PCB | Status | Issues |
|---|---|---|---|---|---|
| A | 5 | Via_SE_Top_L3_MMPX_40 | 4 | done | L3 pad mis registration – 1.4mil |
| A | 5 | Via_SE_Top_L3_MMPX_40 | 13 | done | L3 pad mis registration – -2.45mil |
| A | 7 | Via_SE_Top_L5_MMPX_40_BD20_BL6 | 1 | done | Meas L6 void 36-6mil, 37 – 13.5, designed L6 void 28 |
| A | 7 | Via_SE_Top_L5_MMPX_40_BD20_BL6 | 2 | broken | via misregistered in X and Y direction Meas L4 void 32-18.5mil, 33 – 3, designed L5 void 28 |
| A | 11 | Via_SE_Top_L8_MMPX_40_landless_L9 | 2 | broken | via misregistered in X and Y direction . Pad shift 6mil. Apad l6 7mil. Pad on L9 |
| A | 11 | Via_SE_Top_L8_MMPX_40_landless_L9 | 3 | done | Via misregistered 3mil, Apad sizes Pad on L9 |
| B | 5 | Via_SE_Top_L3_MMPX_40 | 15 | done | Via misregistration 2.3mil |
| B | 5 | Via_SE_Top_L3_MMPX_40 | 22 | done | Via misregistration 1mil, pad misregistration 2.6mil |
| B | 7 | Via_SE_Top_L5_MMPX_40_BD20_BL6 | 15 | done | Apad L2 1.5mil Via 1.25 Apad L4 2.8mil Pad L5 1.1mil Apad L6 1.3mil |
| B | 7 | Via_SE_Top_L5_MMPX_40_BD20_BL6 | 22 | done | Apad L2 1.7mil Via 1.8mil Apad L4 2mil Pad L5 3mil Apad L6 2.3mil |
| B | 11 | Via_SE_Top_L8_MMPX_40_landless_L9 | 15 | done | Pad L8 misregistration ~2mil |
| B | 11 | Via_SE_Top_L8_MMPX_40_landless_L9 | 20 | done | Pad L8 misregistration ~2mil |
| B | 17 | Via_SE_Top_L17_MMPX_40_landless_Bot | 15 | done | 2.6mil misregistration on layer 4 |
| C | 17 | Via_SE_Top_L17_MMPX_40_landless_Bot | 2 | done | L4 7mil Apad misregistration |
| C | 17 | Via_SE_Top_L17_MMPX_40_landless_Bot | 3 | done | L2, L4, L16, L17 pad 5-6mil Apad misregistration |
| C | 17 | Via_SE_Top_L17_MMPX_40_landless_Bot | 4 | done | |

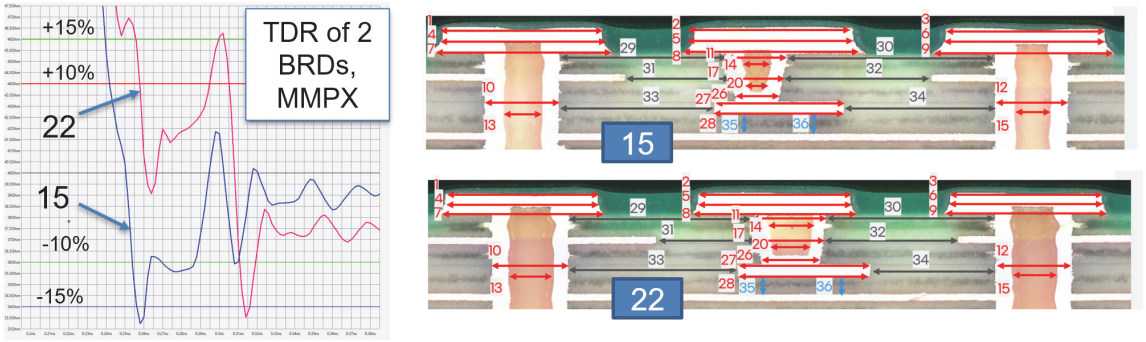



Fig. 16. TDRs of vias to layer L3 for two worst-case boards from vendor A (left plots) and corresponding cross-sections (right pictures).

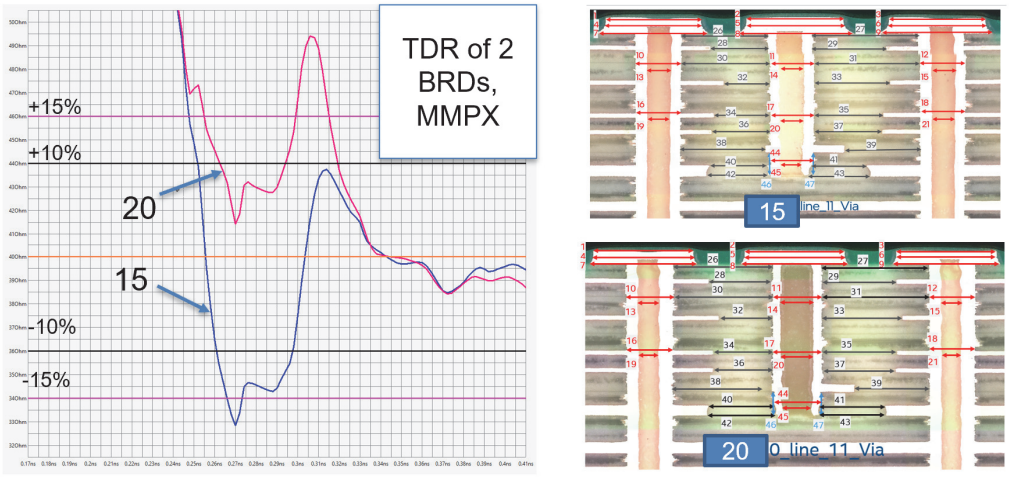



Fig. 17. TDRs of vias to layer L8 for two worst-case boards from vendor B (left plots) and corresponding cross-sections (right pictures).

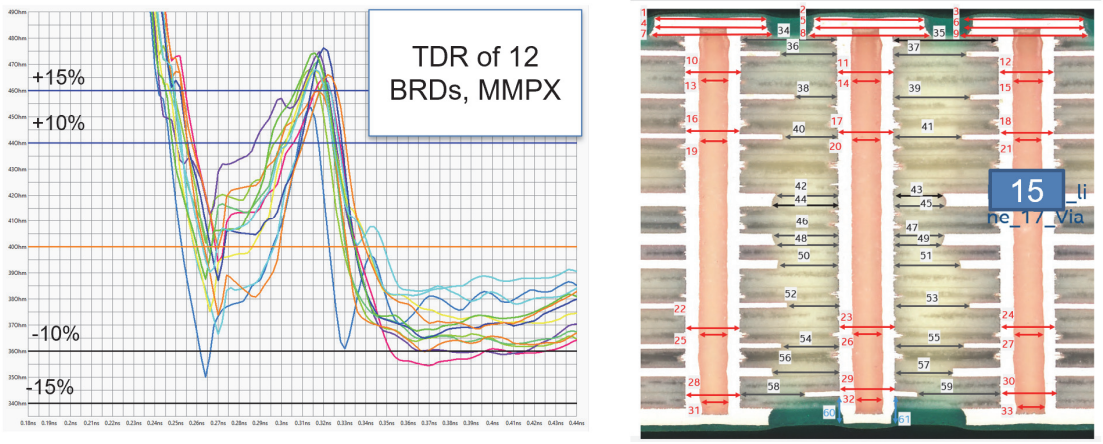



Fig. 18. TDRs of vias to layer L17 for 12 boards from vendor A (left plots) and cross-section of the worst case (right pictures).

What additional insights can we gain from these cross-sections shown in Fig. 16-18? **Misregistration, sharp edges of the anti-pads, variations in signal via barrel diameter, and metal whiskers on the signal via barrel can all significantly alter the via capacitance**. As demonstrated in the next chapter, via parameters are much more sensitive to the via diameter (and any features on the barrel) compared to the dielectric constant. This potential increase in capacitance may be indistinguishable from the anisotropy of the layered dielectric. The increase in via capacitance observed in [36, 37] has been attributed to dielectric anisotropy without additional verification through cross-sectioning of the vias. It is important to note that the dielectrics of advanced PCB laminates are generally homogeneous, and the unexplained capacitance increase may be attributed to geometric discrepancies such as those observed here.

# Waveguide Design Approach

From our reality observations, the primary issue was the layer misregistration, which alters the positions of antipads relative to the signal via barrel, significantly affecting via performance. Can we improve this? Is it feasible to eliminate antipads, or at least reduce the sensitivity of vias to antipad positions caused by misregistration? Additionally, can we define via geometry in a way that eliminates the need for optimization for each layer?
Here are additional design goals based on the reality observations:

- **Reduce sensitivity to manufacturing variations.**
- **Ensure the geometry is simple and usable for any layer.**

To avoid redesigning vias for each layer, we can use the domain decomposition [27] or zones [28] approach. A via is divided into a re-usable middle section and either a vertical-to-horizontal transition (VHT) for a via-to-trace section or a vertical-to-vertical transition (VVT) for a via-to-connector or via-to-BGA section. All three sections can be designed independently with appropriate transmission line ports at their boundaries. This approach is similar to regular decompositional electromagnetic analysis [17].

To ensure the middle section geometry is suitable for any layer, the via must resemble a transmission line or waveguiding structure as closely as possible. The coax vias invented in 1997 [31] are a good fit with some additional requirements for antipads. To avoid confusion with coaxial vias [38], we can refer to this via as a substrate integrated coaxial waveguide (SICW). The concept is similar to converting a rectangular waveguide into a substrate integrated waveguide (SIW) [39]. First, the outer conductor of the coaxial is replaced by stitching vias. Equations defined for coaxial waveguide (CW) and SIW can be used to define SICW, as shown in Fig. 19. Second, **making the antipad diameter equal to an effective coaxial waveguide diameter D transforms the via into a waveguiding structure that is almost independent of the planes**. The similarity of power flow density between SICW and CW is illustrated in Fig. 20.

The localization of SICW depends on the number of stitching vias and distance between them $s$. as recommended for SIW [39], $s$ should be smaller than 0.4 of wavelength in dielectric $\lambda$, to reduce the leaks. Though, the localization should be also verified with the dissipated power metric, that is usually more restrictive condition. **The effective coaxial diameter D**, computed as shown in Fig. 19, defines the cutoff frequency $f_{cutoff}$ for the first high order mode TE11. **The cutoff frequency defines the single-mode bandwidth of the SICW.** It is 96.4 GHz for SICW with Dk = 3, Dvia=8mil, Dst=40mil, Nst=6, s=21mil. In [34] authors recommended distance to stitching vias $0.5D < 0.29\lambda$. It gives via bandwidth about 100 GHz, that is close to the single-mode bandwidth estimate provided here. Note that via is localized even above 96 GHz, but is not functional as we will see in the analysis of via transition to strip line. **To increase the bandwidth, the SICW should be smaller.** For instance, for Dk = 3, Dvia=4mil, Dst=20mil Nst=8, s=7.8mil, the TE11 cutoff frequency is about 199 GHz. That may be sufficient for data rates up to 400 Gbps.

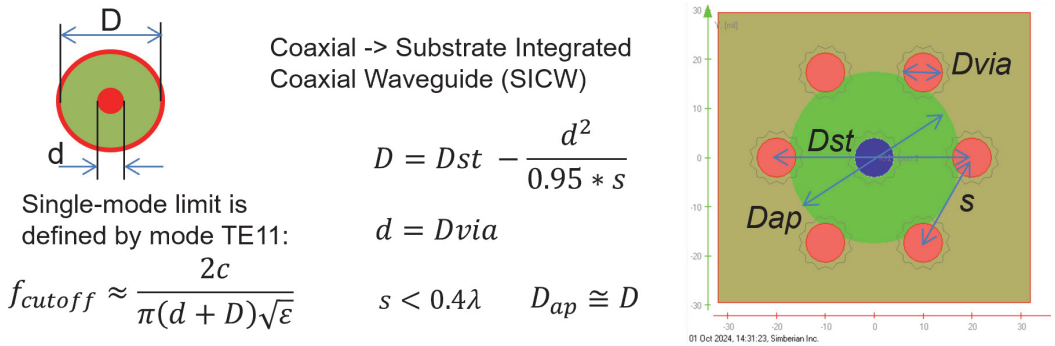



Fig. 18. Similarity of coaxial waveguide and substrate integrated coaxial waveguide and equations to evaluate the effective diameter (D) and single-mode bandwidth.

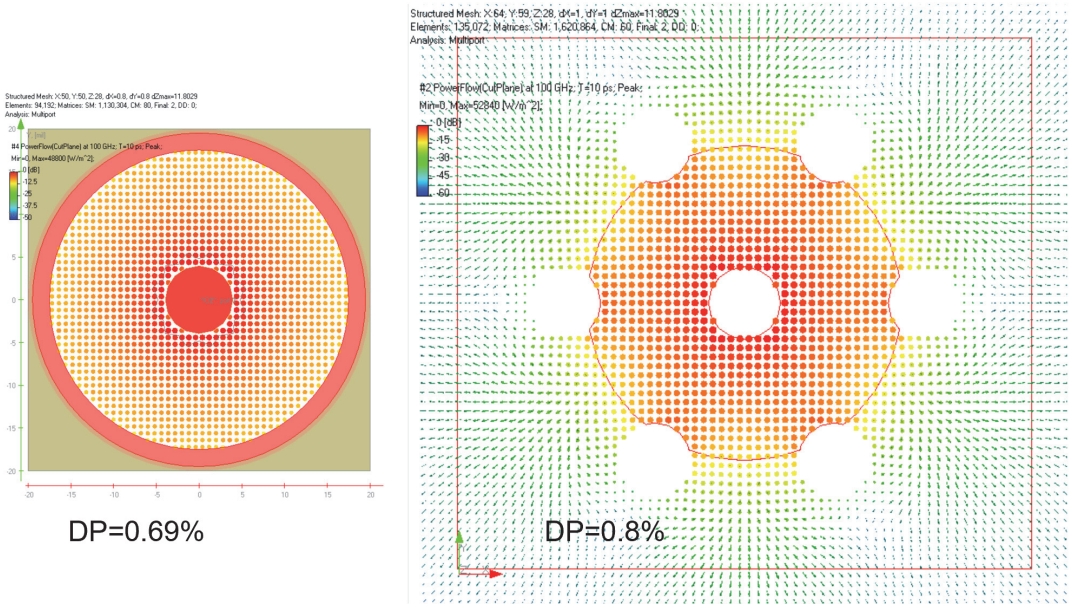



Fig. 20. Comparison of peak PFD in coaxial waveguide and SICW with equivalent diameter at 100 GHz.

Now, let's investigate the sensitivity of SICW to dielectric constant and geometry variations and make sure that it satisfies our low-sensitivity requirement. To verify the sensitivity of SICW, we can use analytical expression for coaxial waveguide impedance $Z_o \approx \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * ln\left(\frac{D}{d}\right)$. Here $d$ is the via diameter and $D$ is the effective diameter as defined in Fig. 19. Change of impedance due to change in dielectric constant $\Delta\varepsilon$ can be expressed as follows: $\Delta Z_o \approx -\frac{\Delta\varepsilon}{2\varepsilon} * Z_o$. 10% change in $\varepsilon$ or Dk produces only about 5% change in the impedance (equivalent to -32dB in RL). Variations of dielectric constants in stackups from Fig. 12 are withing 5%. Considering the effective coaxial diameter $D$ that is also equal to the antipad size, small change $\Delta D$ cause the following change in impedance: $\Delta Z_o \approx \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * \frac{\Delta D}{D}$. The sensitivity to this parameter is also relatively small, because of large $D$. For instance, 1mil change in $D$=40mil can cause only 1 Ohm change in the impedance (equivalent to -40dB in RL). Finally, change in via diameter $\Delta d$ changes the

via impedance as follows: $\Delta Z_o \approx -\frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}} * \frac{\Delta d}{d}$. Here $d$ is small and because of that the via impedance is much more sensitive to it. For instance, 1mil change in via diameter $d$=8mil can cause about 4.3 Ohm change in the impedance (about 27.7dB in RL). This is 5 times more sensitive than the sensitivity to the outer diameter of SICW in this case. Similar high sensitivity of via parameters to via diameter was observed in [40] and in [18]. In addition to misregistration of small antipads, this may be the major souse of the via impedance discrepancies.

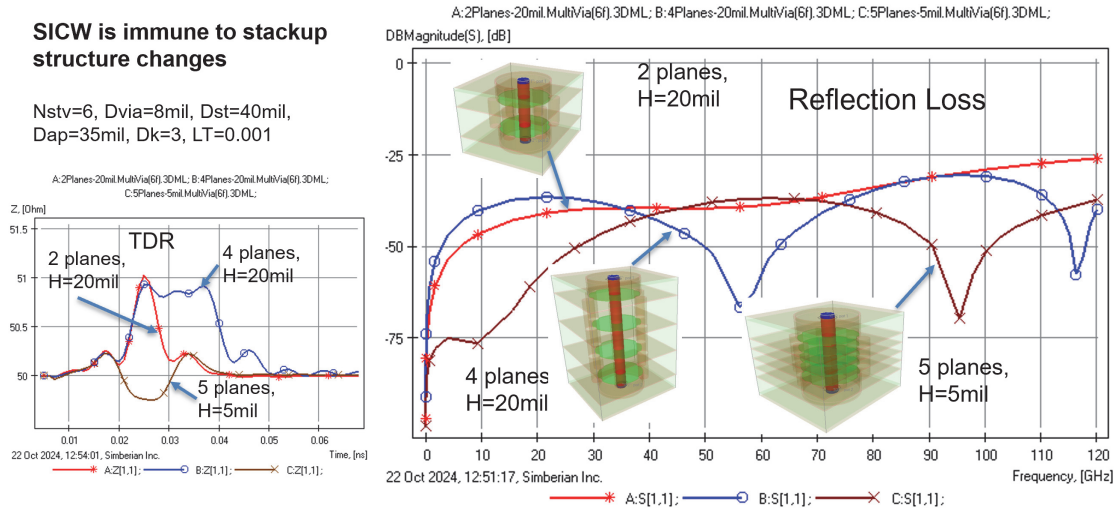



Fig. 21. Reflection loss for three SICW configurations (right plots) and corresponding TDRs (left plots).

To validate SICW sensitivity to inter-plane distance and number of planes, we have simulated three SICW with different number of planes and distances between the planes – the results are show in Fig. 21. De-embedded coaxial ports are used here at the top and bottom of vias. Simbeor 3DML solver with the capacitive ABC is used for the analysis – it produces simultaneously frequency-continuous and time-domain responses of vias. As we can see, the planes change the effective impedance of the SICW, but the range of change is acceptable to fit a large range of stackups. Note that the impedance for SICW without planes should be selected slightly above the target value (about 1 Ohm in this case). So that the planes further reduce it and bring closer to the target.

So far, we have provided the methodology to design the middle section of single-ended via as a SICW. To complete a via design, we need either VVT transition from a connector and/or VHT transition to a stripline. Design of VVT transition from a coaxial connector is quite straightforward. The reflections can be effectively minimized by keeping the same impedance and close geometry at the transition area. TEM wave of the coaxial can be seamlessly matched with the quasi-TEM wave of SICW. Design of VHT for bandwidth up to 100GHz is more challenging. We need to match two modes with different field structure – quasi-TEM in SICW and quasi-TEM of either stripline or coplanar stripline as shown in Fig. 22. There is always relatively large transition or bend area between the lines with two modes – this area works as a mode transformer. In any case, to reduce the reflections we need to keep the impedance of the transition area as close to the target as possible. Three examples of VHT are shown in Fig. 22 together with TDRs and magnitudes of reflection and insertion losses. Configuration #1 is the simplest,

#2 is more realistic and #3 is the best, but it may be difficult to manufacture. Better match is possible, but it will complicate the structure and make it more sensitive to geometry variations. Notice that the best VHT #3 is neither inductive, nor capacitive due to the resonance in the transition area around 110 GHz – this is right above the via single-mode bandwidth.

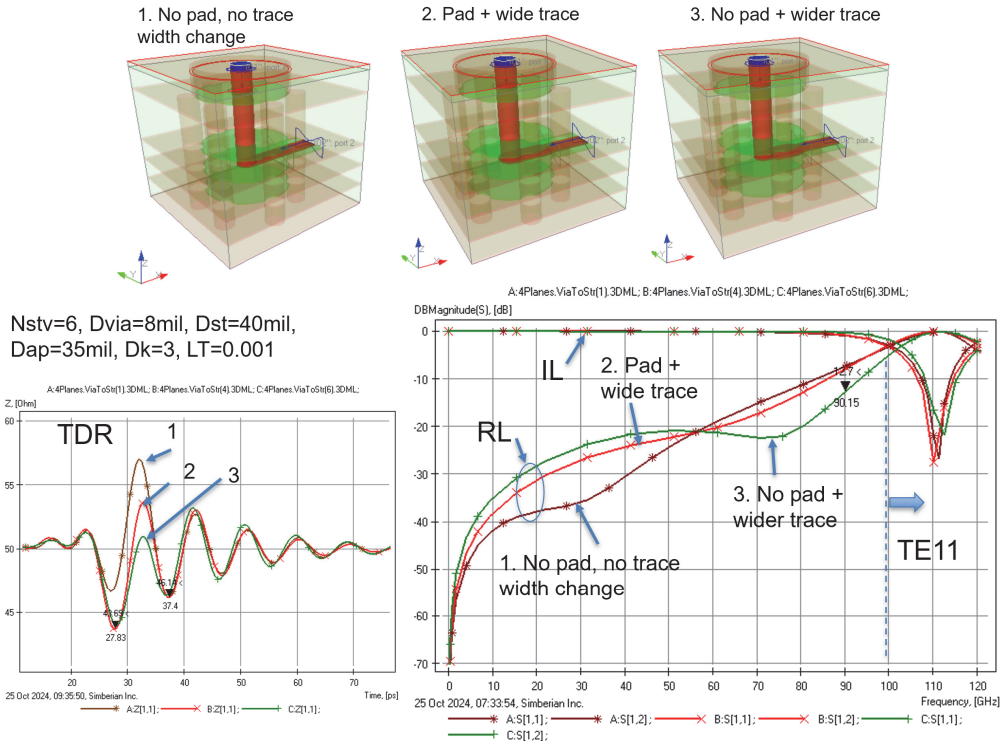



Fig. 22. Three possible VHT from stripline to SICW (top pictures) and corresponding TDR (left plots) and RL and IL (right plots).

Fig. 23 illustrates the fields in VHT at 110 GHz. As we can see from the electric field distribution, the quasi-TEM mode is transformed into an almost perfect TE11 mode (electric field points into via on the right side and out of via on the left side). As we can also see from the PFD, the energy flows on two sides of via have opposite directions. The coplanar stripline mode is transformed into TE11, that is reflected at the top boundary and transformed back to TEM mode here. It looks like a resonance, but it is mode transformation with reflection of TE11. Is it possible to avoid the mode transformation? In [20] authors used every layer interconnect (ELIC) technology to create a circular waveguide resonator under the transition, to extend the via bandwidth. Though, the benefits are not obvious and it also violates our simplicity requirement. Note that the TE11 can be transformed back to TEM with another complimentary transition to stripline – this should work similar to the mode transformation at complimentary turns of differential traces. **A simpler solution is to make everything smaller.** Reducing via diameter to 4mil and stitching circle diameter to 20mil increases the bandwidth of VHT up to 120 GHz as demonstrated in Fig. 24. This is the simplest configuration with pad and transition to relatively wide (8mil) coplanar stripline (wider trace is used to reduce the losses).

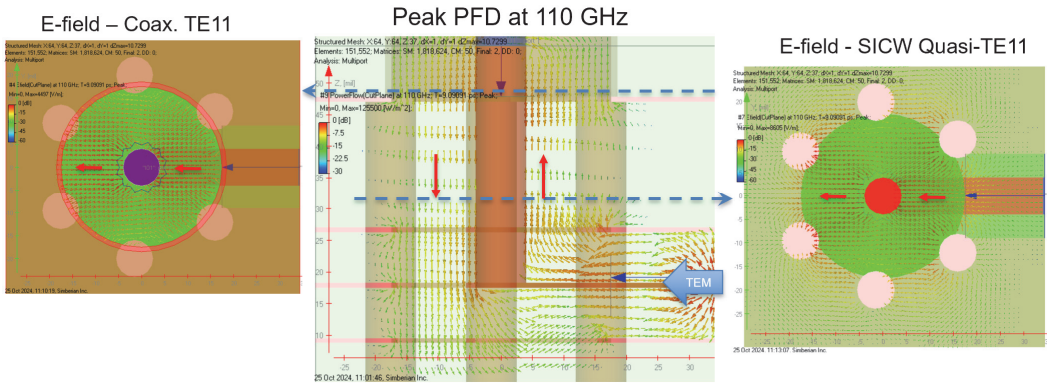



Fig. 23. Peak PFD at 110 GHz with unit stripline excitation (middle picture) and peak of electric field distribution in SICW section (right plot) and in the coaxial section (left plot).

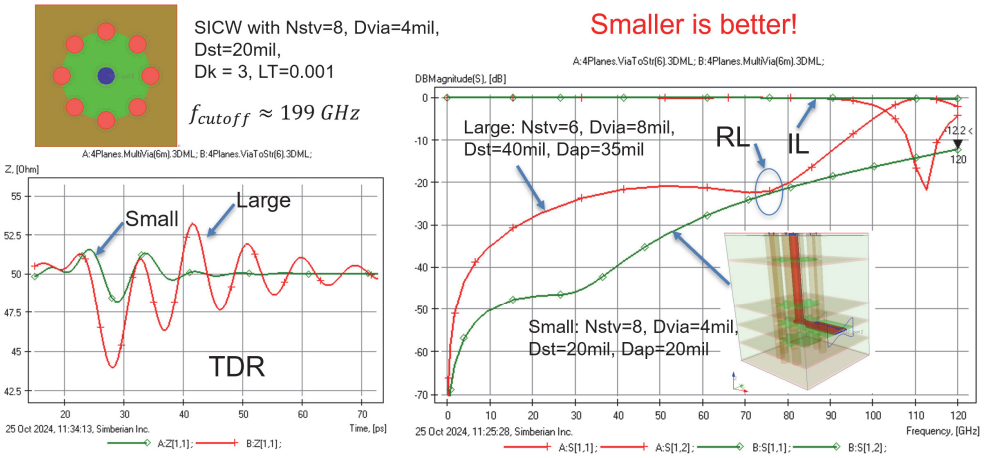



Fig. 24. VHT design with bandwidth above 120GHz. TDR is on the left plot and RL, IL are on the right plot (green lines). Results from Fig. 22 for configuration 3 are also plotted as red curves.

The SIW design approach to single-ended vias can be applied to differential vias as well. **We can use twinax cable [42] as a prototype for construction of a substrate integrated twinax waveguide (SITW) for a middle section of differential via.** The approach is the same as with conversion of CW into SICW – replace the outer conductor with stitching vias to reduce leaks as in SIW and make large antipads with the effective size of the waveguiding structure. **Stitching vias are the essential part of the differential via waveguiding structure.** Example of SITW design that is relatively independent of the number of planes and inter-plane distance is shown in Fig. 25. Corresponding TDRs and RLs demonstrating relative immunity to planes are shown in Fig. 26. The target impedance here is 85 Ohm and the impedance of SITW without planes is about 87.5 Ohm. Planes with smaller distances slightly reduce the impedance as we can see from TDR in Fig. 26. We can conclude that SITW can be used as the any-stackup via. The critical design parameters for SIW are via diameter (Dvia), distance between signal vias (Dvv) and distance to stitching vias (Hstv). In this example we have used oval pattern with 8 stitching vias.

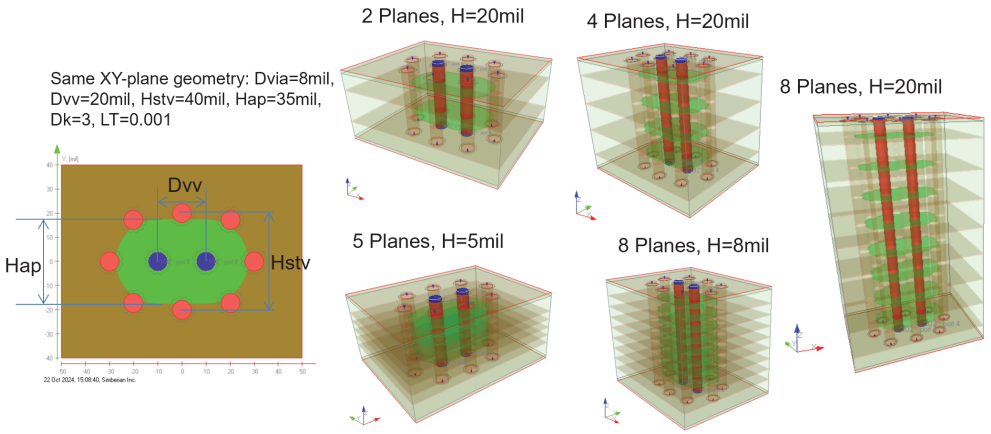



Fig. 25. Five configurations of SITW with the same geometry in XY-plane.

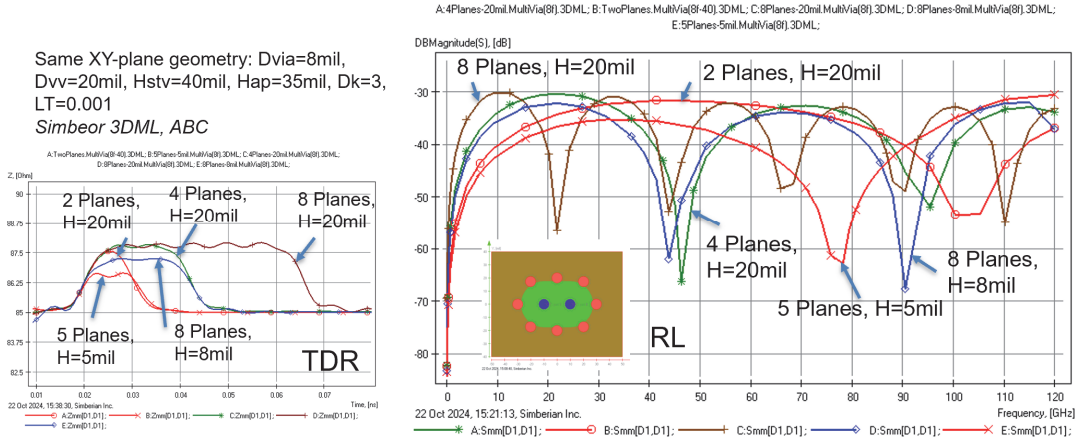



Fig. 26. TDRs (left plots) and reflection loss (right plots) for five SITWs shown in Fig. 25.

Use of SITW as the middle section of via is just a part of the problem. The transitions (VVT and VHT) are also required. A rectangular grid pattern with 10 stitching vias may be used for a seamless transition to BGA or connector pins. Though, the BGA balls may be unavoidable and relatively large discontinuity. Considering VHT, as in case of single-ended vias, it may be the most challenging part of a differential via design. Examples of two transitions from differential vias to differential traces are provided in Fig. 27. VHT #1 is the simplest straightforward connection and #2 is a transition with attempt to compensate the pad-to-pad capacitance. Though, the vias remain capacitive and the high-order modes restrict the vias bandwidth to about 97 GHz. Comparing to SICW, transition to differential traces requires more space between the stitching vias. It creates a gap between stitching vias that reduces the localization and increases the leaks similar to the single-ended case observed in [43]. A loosely coupled breakout may be considered. Though, the alternative solution is to make it smaller.

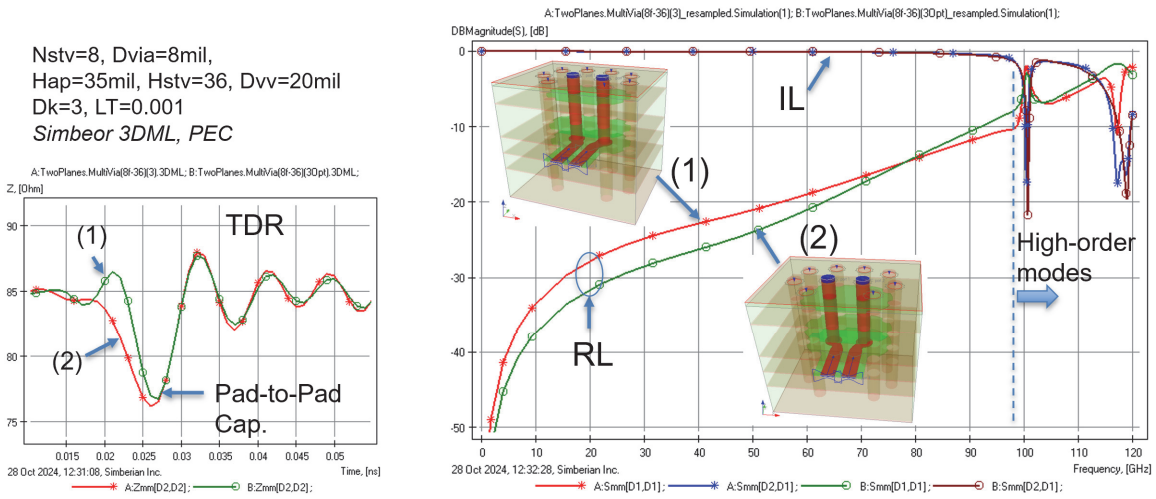



Fig. 27. TDRs (left plot) and RL, IL for two VHT from SITW to coplanar differential stripline – the simplest (1) and with impedance adjustment (2).

# Conclusion

In this paper, we have introduced a novel approach to the design and optimization of PCB vias for high-speed applications ranging from 112 to 224 Gbps. Our investigation into the physics of vias has identified the critical conditions and metrics necessary for effective localization within a single-mode bandwidth up to 120 GHz. To address the sensitivity of vias to stackup adjustments, we proposed two approaches. The first approach based on simultaneous optimization, resulted in via geometries that were overly sensitive to manufacturing variations. To overcome these challenges, we proposed the design of any-stackup vias using waveguiding structures similar to substrate integrated waveguides, specifically substrate integrated coaxial (SICW) and twinax (SITW) waveguides. This design is further simplified by segmenting the vias into middle sections and transitions. Our findings demonstrate that the middle sections of SICW and SITW are relatively independent of the stackup structure. While the waveguiding approach is still a work in progress, we plan to test it further in practical scenarios. Our work bridges the gap between theoretical designs and real-world implementations, offering a robust and simple methodology for designing vias that are less sensitive to manufacturing variations and stackup adjustments.

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