

Building advanced transmission line and via-hole models for serial channels with 10 Gbps and higher data rates DesignCon IBIS Summit, Santa Clara, February 7, 2008

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Agenda

- Introduction
 - De-compositional analysis of multi-gigabit channels
- Building models for transmission lines
 - Proximity, edge and skin-effects
 - Surface roughness
 - Metal plating
 - Dielectric polarization and high-frequency dispersion and loss
- Building models for differential via-holes
 - Localizability
 - De-embedding
 - Effective via-hole impedance and geometry optimization
- Conclusion



Introduction

- Faster data rates drive the need for accurate electromagnetic models for multi-gigabit data channels
- Without the electromagnetic models, a channel design may require
 - Test boards, experimental verification, ...
 - Multiple iterations to fix or improve performance...
- No models or simplified static models may result in complete failure of the design



Major signal degradation factors





Electromagnetic models for interconnects





De-compositional system-level analysis





Hybrid simulation technology is used to illustrate this presentation

Method of Lines (MoL)

- More accurate than finite element method (FEM) and finite integration technique (FIT) for problems with multiple thin dielectric and metal layers
- Provides conductor interior solution for metal planes
- Trefftz Finite Elements (TFE) or Ultra-Week Discontinuous Galerkin's Element (UWDG)
 - Can be used for any material and easy to interface with MoL
 - Used to model strip conductor interior with rough surface
- Method of Simultaneous Diagonalization (MoSD)
 - Extracts modal and per unit length parameters of lossy multiconductor lines and periodic structures
 - Allows precise non-reflective de-embedding
 - Provides 3D observable definition of the characteristic impedance



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Conductor attenuation and dispersion effects



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Current distribution in rectangular conductor



t/s is the strip thickness to the skin depth ratio

Jc/Je is the ratio of current density at the edge to the current in the middle.



Transition to skin-effect and roughness

Transition from 0.5 skin depth to 2 skin depth for copper interconnects on PCB, Package, RFIC and IC



Interconnect or plane thickness in micrometers vs. Frequency in GHz

Ratio of skin depth to r.m.s. surface roughness in micrometers vs. frequency in GHz



Roughness has to be accounted if rms value is comparable with the skin depth



Modeling roughness with the effective surface impedance

Rough surface may be characterized with two parameters and approximated as triangular bumps along the current flow



Effect of surface roughness on a PCB micro-strip line parameters

7 mil wide and 1.6 mil thick strip, 4 mil substrate, Dk=4 (lossless), 2-mil thick plane. Strip and plane are copper. Metal surface RMS roughness 1 um (plane and bottom surface of strip), rms roughness factor 2,



25 % loss increase at 1 GHz and 65% at 10 GHz





Transition to skin-effect and roughness in a package strip-line

79 um wide and 5 um thick strip in dielectric with Dk=3.4. Distance from strip to the top plane 60 um, to the bottom plane 138 um. Top plane thickness is 10 um, bottom 15 um. RMS roughness is 1 um on bottom surface and almost flat on top surface of strip, RMS roughness factor is 2.



Transition is up to 2 GHz, 33% loss increase at 10 GHz

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Effect of RoHS metal surface finish on a PCB micro-strip line parameters

70

65

60

55

50



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NoFinish – 8 mil microstrip on 4.5 mil dielectric with Dk=4.2, LT=0.02 at 1 GHz.

ENIG2 - microstrip surface is finished with 6 um layer of Nickel and 0.1 um layer of gold on top Nickel resistivity is 4.5 of copper, mu is 10

 \sim 50% loss increase from 0.1 to 10 GHz



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Dielectric attenuation and dispersion effects

- Dispersion of complex dielectric constant
 - Polarization changes with frequency
 - High frequency harmonics propagate faster
 - Almost constant loss tangent in broad frequency range – loss ~ frequency
- High-frequency dispersion due to nonhomogeneous dielectrics
 - TEM mode becomes non-TEM at high frequencies
 - Fields concentrate in dielectric with high Dk or lower LT
 - High-frequency harmonics propagate slower
 - Interacts with the conductor-related losses



Broadband causal dielectric models with dispersion are required

With one measurement of Dk and LT for PCBs the possibilities are 1) Flat non causal (FlatNC) model



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Djordjevic, R.M. Biljic, V.D. Likar-Smiljanic, T.K.Sarkar, IEEE Trans. on EMC, vol. 43, N4, 2001, p. 662-667.

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Effect of dielectric models on a PCB micro-strip line parameters



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FlatNC – 7 mil microstrip on 4.0 mil dielectric with Dk=4.2, LT=0.02 and without dispersion

1PD – same line with Dk=4.2, LT=0.02 at 1 GHz and 1-pole Debye dispersion model

WD – same line with Dk=4.2, LT=0.02 at 1 GHz and wideband Debye dispersion model

No metal losses to highlight the effect



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Building transmission line models with a field solver

Effect or Feature \ Solver	2D Static Solvers	2D Quasi-Static Solvers	2.5D MoM Solvers	3D FEM Solvers	3D FDTD or FIT Solvers
Extracted parameters	C, L, Ro, Go Rs, Gs at 1GHz	L(f), R(f)	S(f), Y(f), Z(f)	S(f), Y(f), Z(f)	S(f), Y(f), Z(f)
P.U.L. RLGC(f)	No	R(f) and L(f)	Νο	Νο	No
Thin dielectric layers	Difficult	Νο	Yes	Difficult	Difficult
Transition to skin-effect	Νο	Yes	No	Difficult	No
Skin and proximity effects	Approximate	Yes with saturation	SIBC	SIBC	Difficult
Metal finishing	No	Difficult	No	No	No
Metal surface roughness	No	No	No	Resistivity adjustment	No
Dielectric dispersion	No	No	No	1 and 2-pole models	1 and 2-pole models
3D impedance	Νο	No	Yes	No	No

SIBC – Surface Impedance Boundary Conditions, works with well-developed skin-effect



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Differential via-holes

 Differential vias are two-via transitions through multiple parallel planes with possible stitching vias nearby



- Two modes propagate independently trough a symmetrical pair
 - Differential (+-) two vias are two conductors: *Id=0.5(I1-I2), Vd=V1-V2*
 - Common (++) two vias one conductor and planes and stitching vias are another conductor: Ic=I1+I2, Vc=0.5(V1+V2)
- Signal in differential pair always contain differential mode (useful) and may contain common mode induced by asymmetries in driver/receiver and by discontinuities



Differential mode in via-holes

Differential mode has two identical currents on the via barrels



- The via-holes can be isolated from the rest of the board for the electromagnetic analysis with any boundary conditions (PEC, PMC, PML, ABC)
 - Distance from the vias to the simulation area boundaries should be large enough to avoid effect of sidewalls
 - In that case, the differential mode S-parameters are practically independent of the boundary conditions



Common mode in differential via-holes going through multiple parallel planes

- Planes are not terminated and the return current for common mode is the "displacement" current between the planes
 - The problem is non-localizable may require analysis of the whole board
- Planes are terminated with the decoupling capacitors and the return current is a combination of the "displacement" currents through capacitors and planes
 - The problem is non-localizable decaps have low impedance only in a narrow frequency band



 Problem can be localized (localizable) and solved with any boundary conditions







Any 3D full-wave solver can be used to generate a model for localizable via-holes



Electromagnetic solver generates Touchstone s4p file with tabulated scattering parameters:



Multiport parameters extraction with de-embedding and reference plane shift



Effect of de-embedding on multiport parameters

Non-reflective excitation ports (lumped or wave-ports) increase the model quality





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Shift of reference planes makes model electrically smaller and reusable



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Estimation of the de-embedding quality

- Analysis of a transmission line segment can reveal de-embedding defects
- Analysis of 25, 50 and 100-Ohm benchmark strip line segments can be used for this purpose

Benchmarks from J.C. Rautio, IEEE on MTT, v.42, N11, 1994, p. 2046-2050.

S-parameters normalized to 25, 50 and 100 Ohm, segment length is 90 deg. at 15 GHz No losses, no dispersion – |S21| must be unit |S11| must be zero





Design of impedance-controlled differential via-holes

- Effective impedance of via can be defined as the normalization impedance with minimal reflection [SD1D1] and maximal transition [SD1D2]
- Optimal via-holes have effective impedance 100 Ohm



Not optimal via-holes can significantly degrade the signal at system-level



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U16

diff receiver

Even the optimal via-holes are not ideal transitions and require models







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6-plane PCB

8-mil vias are 24 mil apart with 32 mil anti-pads and 20 mil pads only in signal layers, traces are 6 mil wide 10 mil apart

The effective impedance of vias is close to 100 Ohm over a wide frequency band

Conclusion: Transmission line models

- Build broadband models for data channels with data rates 10 Gbps and higher
- Use 3D full-wave solvers to extract RLGC(f) matrix parameters per unit length for W-element
- Use broadband and causal dielectric models
- Have conductor models valid over 5-6 frequency decades in general
 - Account for transition to skin-effect, shape and proximity effects at medium frequencies
 - Account for skin, dispersion and edge effects at high frequencies
 - Account for conductor surface finish and roughness



Conclusion: Via-hole models

- Distinguish localizable and non-localizable cases
 - Dependence of S-parameters from the boundary conditions usually shows that the problem is non-localizable
- Only localizable cases can be analyzed with a 3D fullwave solver
 - Differential mode propagation even without stitching vias
 - Common mode propagation only with stitching vias nearby
- Complete board analysis is required to build accurate models for non-localizable cases
 - Hybrid distributed analysis with transmission plane solvers may be the best choice for such problems considering performance and accuracy
 - Localized 3D full-wave differential via analysis can be embedded into the system-level hybrid solution to increase accuracy

