

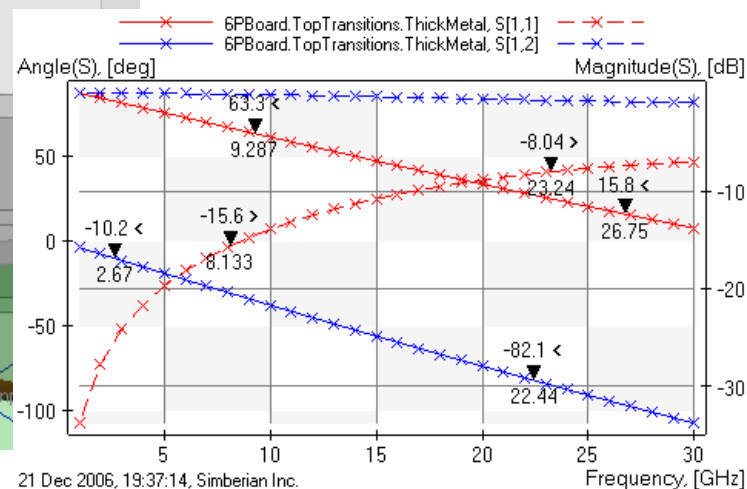
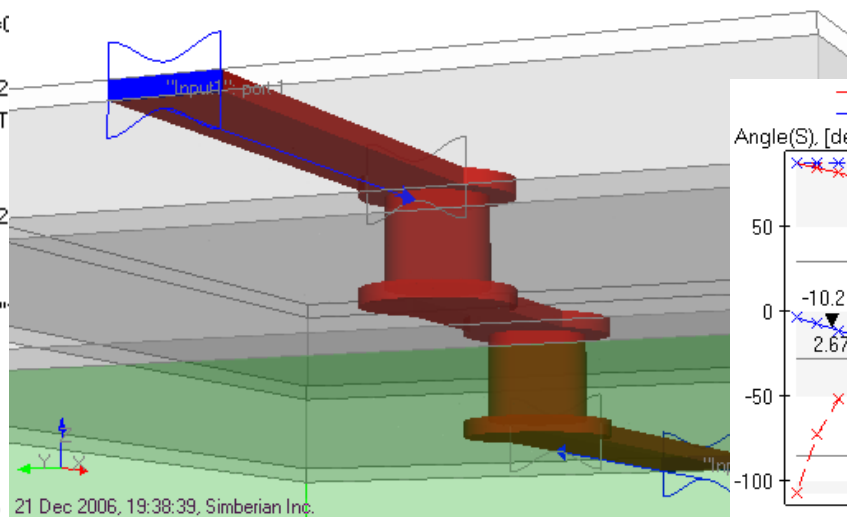
Effect of slots in reference planes on signal propagation in single and differential t-lines

Solution: "MicroVias"

- 6PBoard
 - Materials
 - "copper", RRes=1, Rough=0.01
 - "IdealMetal"
 - "prepreg", DK=4.7, LT=C
 - "Vacuum"
 - "FR4", DK=4.2, LT=0.02
 - StackUp: LU=[mil], NL=15, T
 - TopTransitions
 - CircuitData: LU=[mil]
 - Multiport: 2 inputs, 2
 - LatticeBox
 - Geometry
 - GeoComposite: "
 - TLines
 - Inputs
 - ThickMetal
 - CollapsedMetal
 - BottomTransition
- Graph1(MultiportParameters vs. 21 Dec 2006, 19:38:39, Simberian Inc.)
- Graph2(MultiportParameters vs. Frequency)

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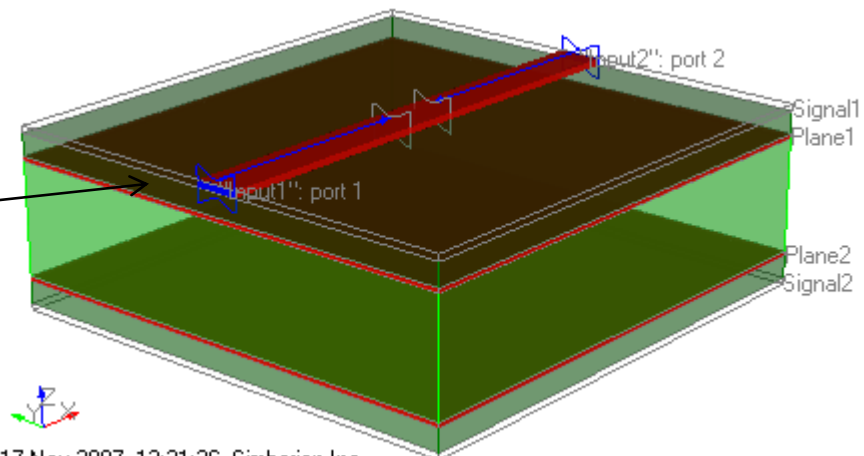
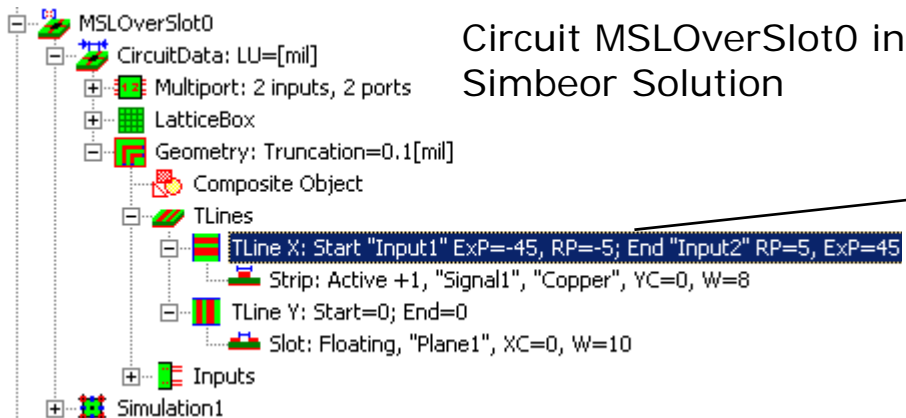
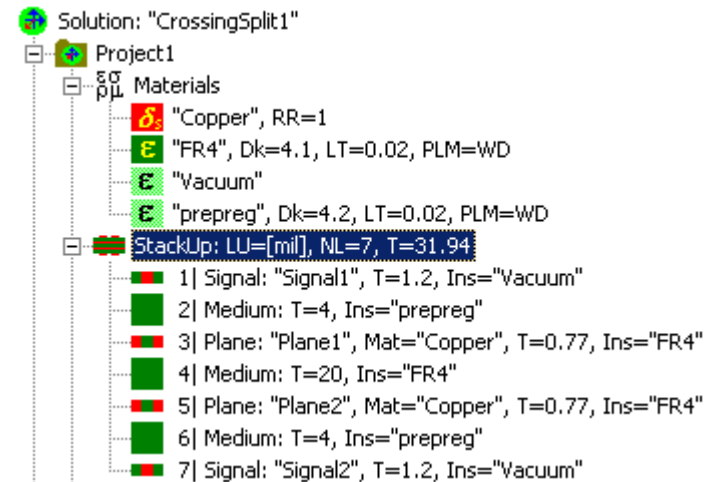
Introduction

- ❑ Routing traces over splits in reference planes may cause significant signal degradation in multi-gigabit data channels
- ❑ To maximize the transition of the signal over the splits and minimize the reflection, stack-up has to be optimized to minimize the effect of the splits
- ❑ This example demonstrates how to use electromagnetic simulator for quantitative analysis of the effect of slot in a reference plane on S-parameters of a small trace segment
- ❑ Simbeor 2007 full-wave 3D solver for multilayered circuits is used to generate the results

Micro-strip line segment (no slot yet)

- Simple 4-layer stackup
- Wideband Debye dispersion and loss models used for the dielectrics
- 8-mil wide micro-strip line segment in the topmost layer "Signal1"

Materials and stackup in Simbeor Solution

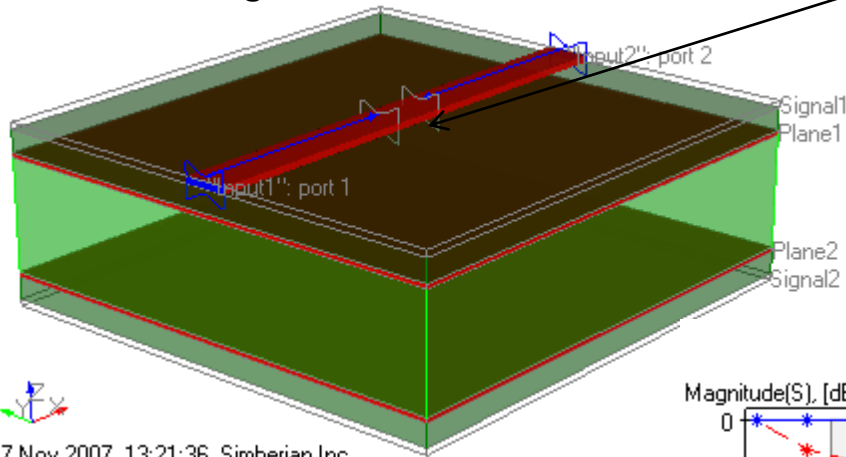


17 Nov 2007, 13:21:36, Simberian Inc.

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S-parameters of a small micro-strip line segment (simulation set-up calibration)

Circuit MSLOverSlot0
SlotLength=0 [mil]

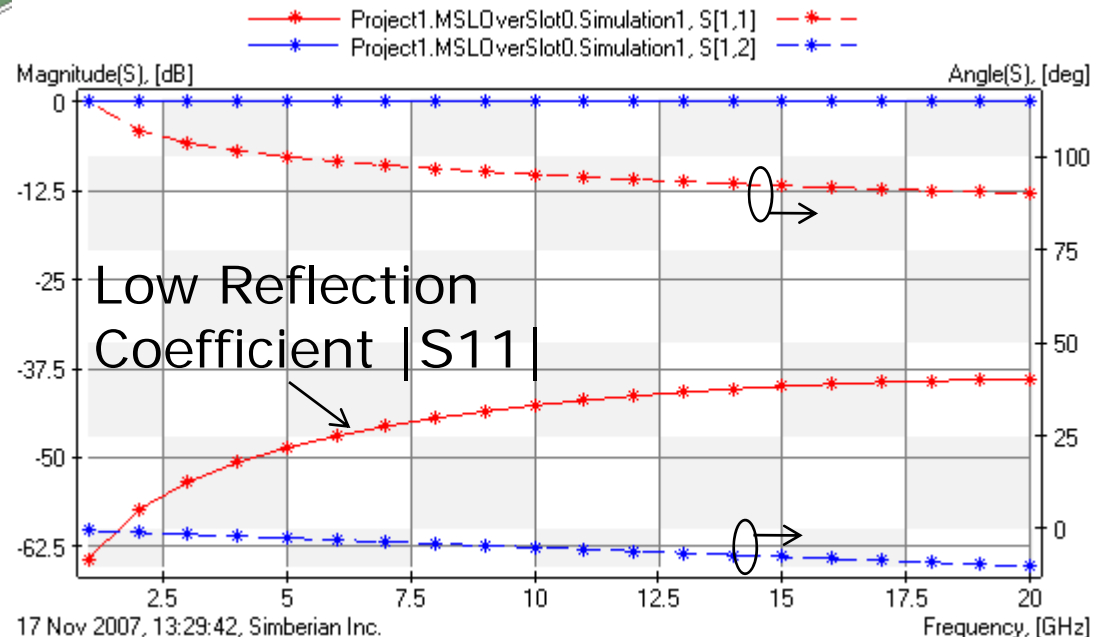


Ports de-embedded to have just 10-mil line segment in the middle (where the slot will be located)



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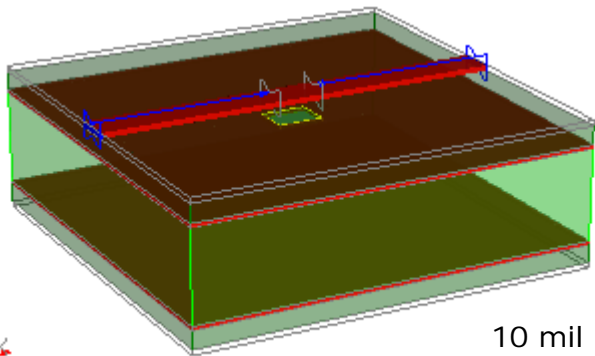
S-parameters are normalized to 50 Ohm and characteristic impedance changes with frequency, that causes increase of reflection at higher frequencies (reaches about -40 dB at 20 GHz)



17 Nov 2007, 13:29:42, Simberian Inc.

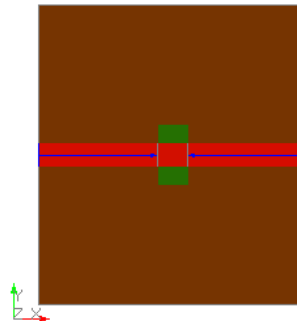
5 circuits with different slot length and slot width 10 mil (size along the t-line)

Circuit MSLOverSlot1
SlotLength=8 [mil]



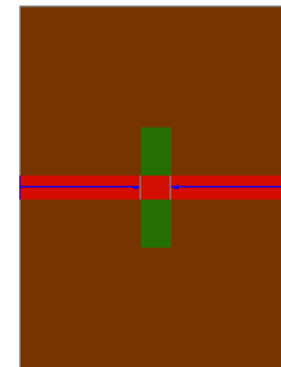
17 Nov 2007, 13:55:29, Simberian Inc.

Circuit MSLOverSlot2
SlotLength=20 [mil]



17 Nov 2007, 13:56:34, Simberian Inc.

Circuit MSLOverSlot3
SlotLength=40 [mil]

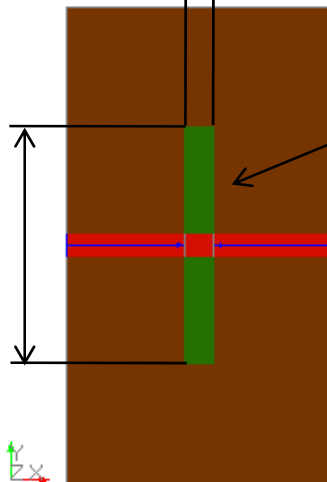


17 Nov 2007, 13:57:08, Simberian Inc.

10 mil in all examples

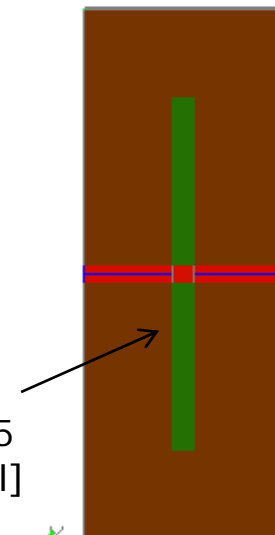
SlotLength is a parameter

Circuit MSLOverSlot4
SlotLength=80 [mil]



17 Nov 2007, 13:57:44, Simberian Inc.
10/7/2008

Circuit MSLOverSlot5
SlotLength=120 [mil]



17 Nov 2007, 13:58:24, Simberian Inc.

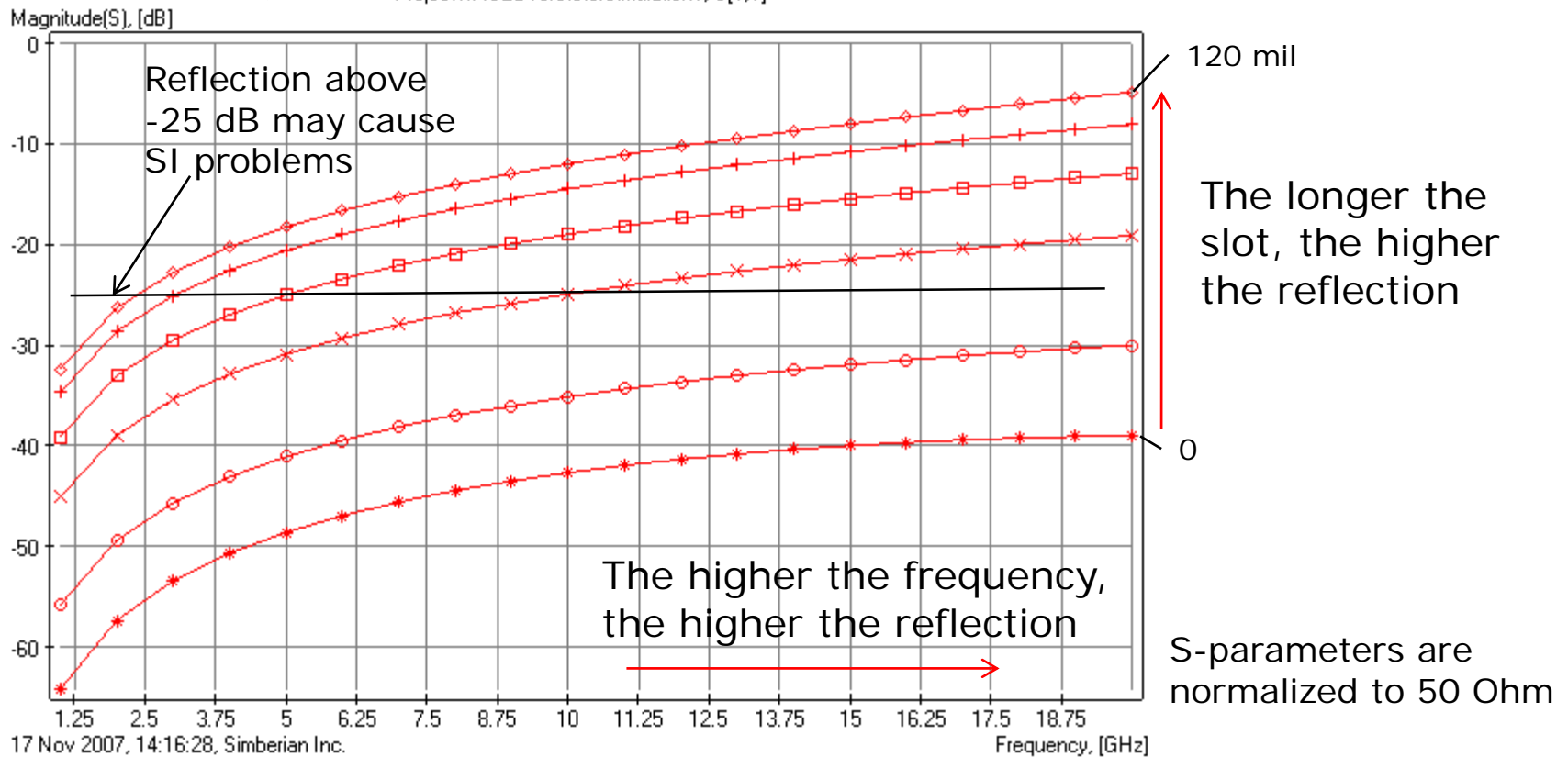
Magnitude of reflection coefficient $|S_{11}|$ for circuits with different Slot Length

SlotLength increases ↓

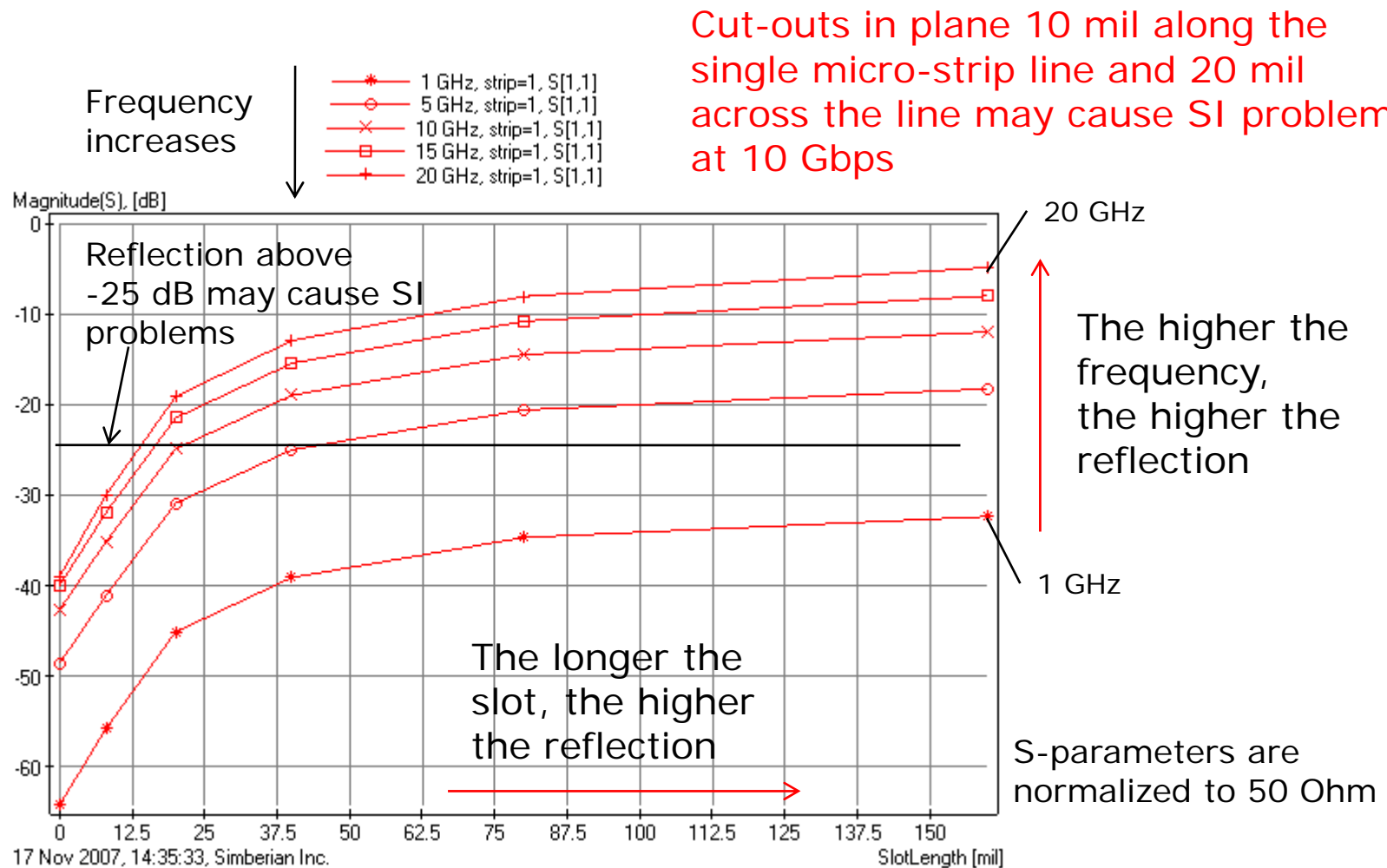
- Project1.MSLOverSlot0.Simulation1, S[1,1]
- Project1.MSLOverSlot1.Simulation1, S[1,1]
- Project1.MSLOverSlot2.Simulation1, S[1,1]
- Project1.MSLOverSlot3.Simulation1, S[1,1]
- Project1.MSLOverSlot4.Simulation1, S[1,1]
- Project1.MSLOverSlot5.Simulation1, S[1,1]

Acceptable reflection loss for a single discontinuity depends on a particular design.
-25 dB selected for this example.

-25 dB selected for this example.

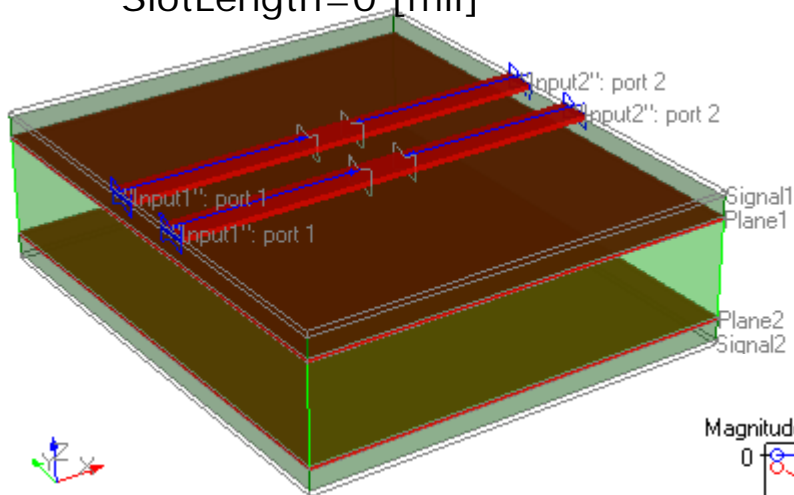


Magnitude of reflection coefficient $|S_{11}|$ as a function of the Slot Length



S-parameters of a small differential micro-strip line segment (simulation set-up calibration)

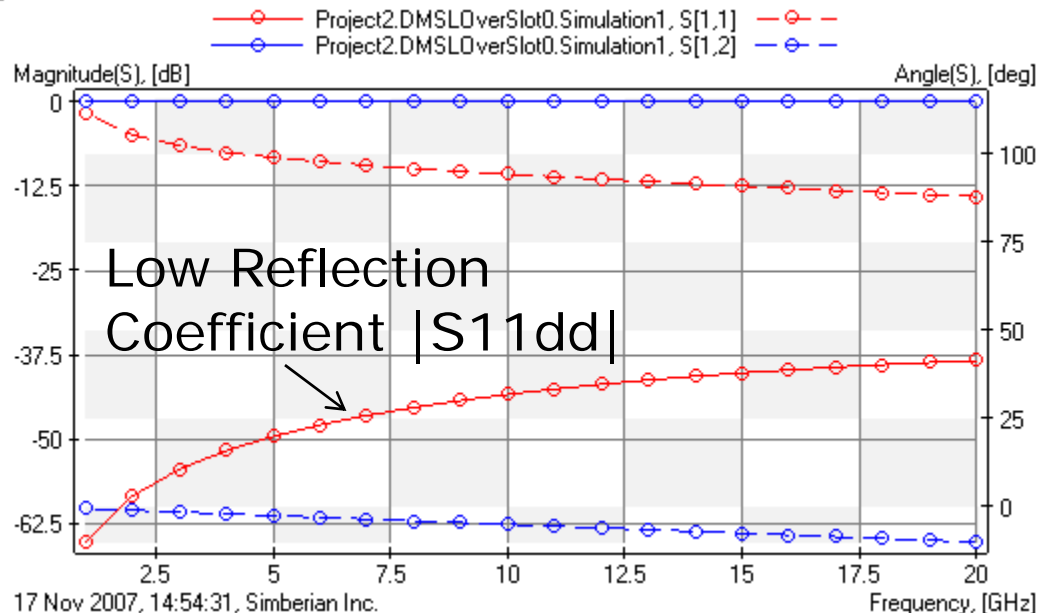
Circuit DMSLOverSlot0
SlotLength=0 [mil]



Two microstrips 7 mil wide and 17.5 mil apart (about 100 Ohm differential impedance).
Ports de-embedded to have just 10-mil line segment in the middle (where the slot will be located)

17 Nov 2007, 14:50:51, Simberian Inc.

Differential to differential S-parameters are normalized to 100 Ohm and characteristic impedance changes with frequency, that causes increase of reflection at higher frequencies (reaches about -40 dB at 20 GHz)



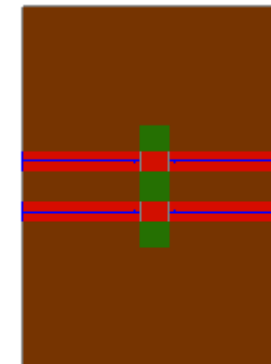
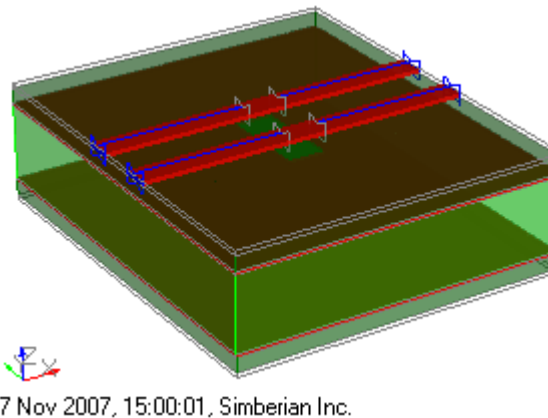
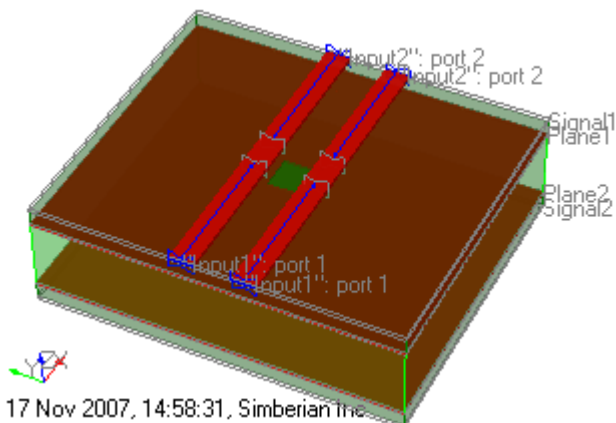
17 Nov 2007, 14:54:31, Simberian Inc.

5 circuits with different slot length and slot width 10 mil (size along the t-line)

Circuit DMSLOverSlot1
SlotLength=10.5 [mil]

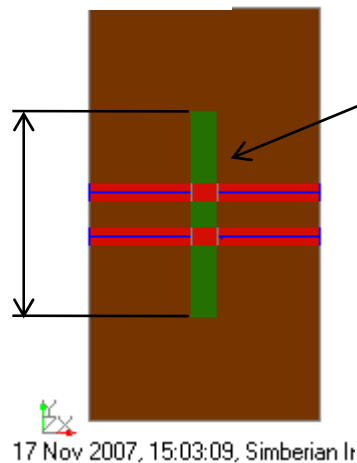
Circuit DMSLOverSlot2
SlotLength=24.5 [mil]

Circuit DMSLOverSlot3
SlotLength=42 [mil]



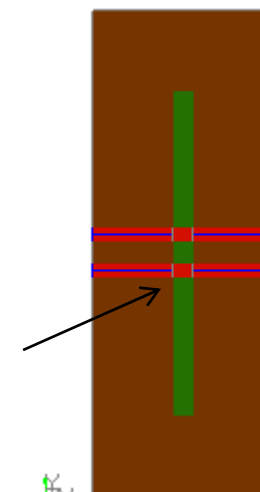
17 Nov 2007, 15:02:26, Simberian Inc.

SlotLength is a parameter



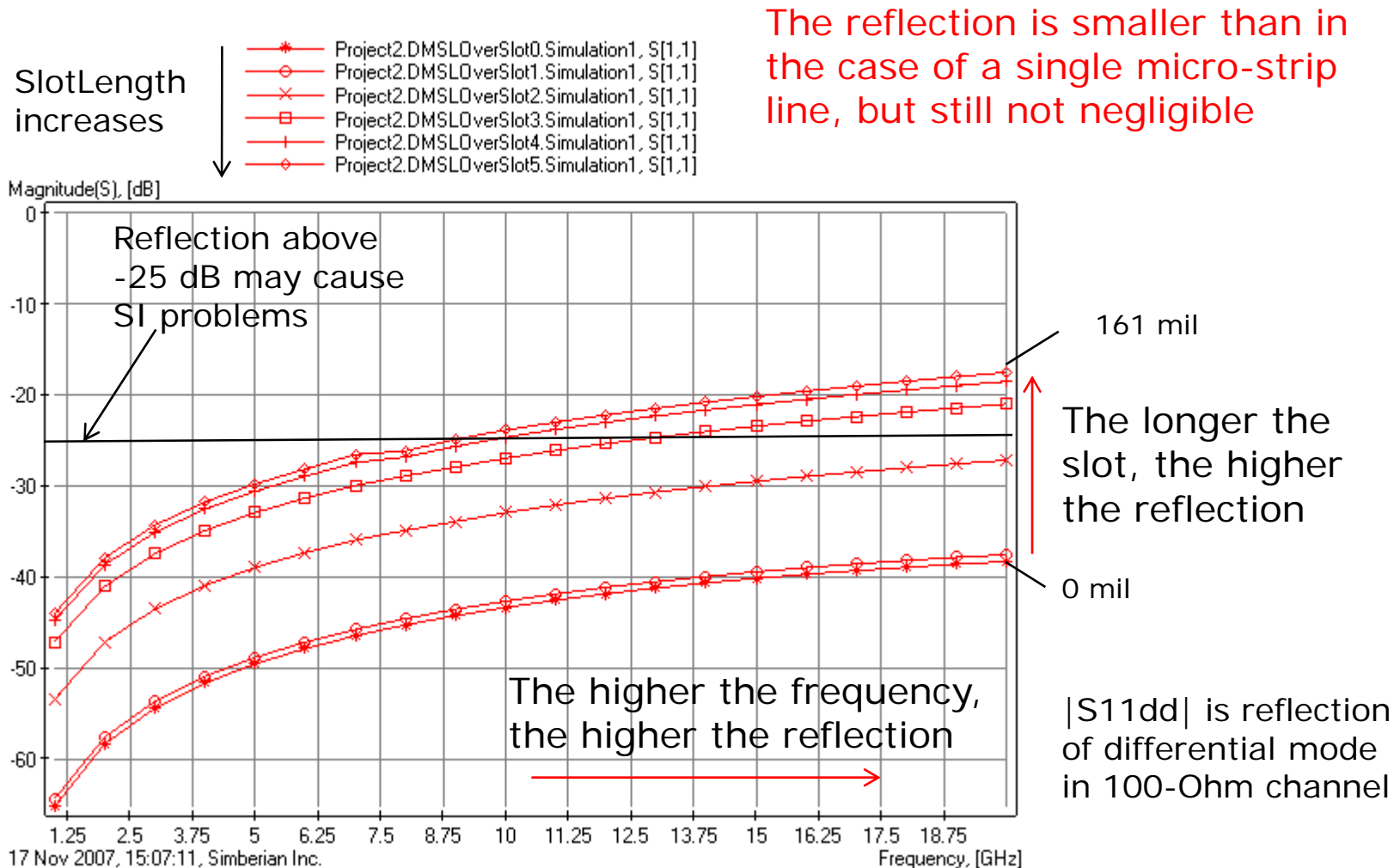
Circuit DMSLOverSlot4
SlotLength=161 [mil]

Circuit DMSLOverSlot5
SlotLength=80.5 [mil]



17 Nov 2007, 15:04:15, Simberian Inc.

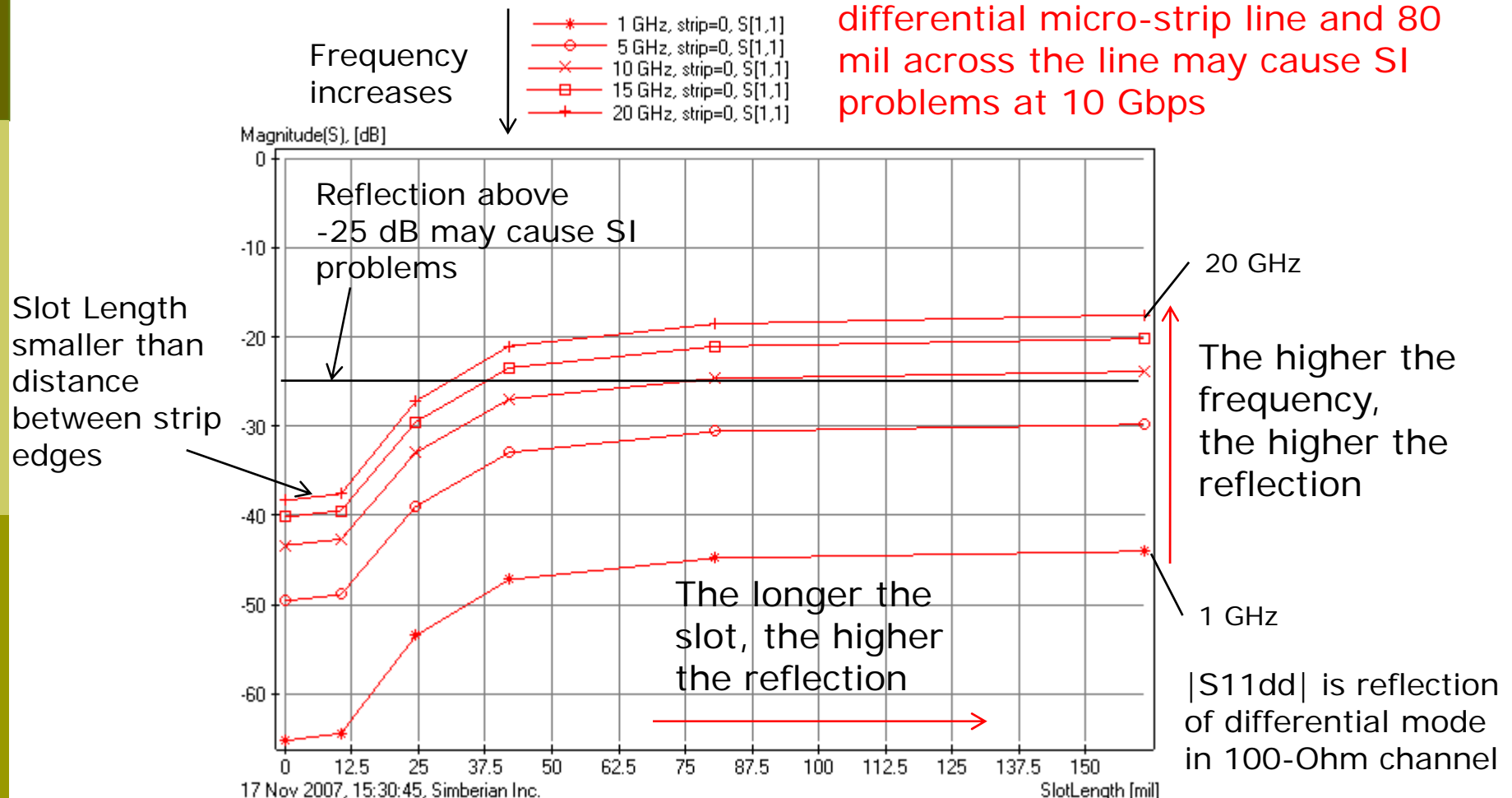
Magnitude of reflection coefficient $|S_{11dd}|$ for circuits with different Slot Length



The reflection is smaller than in the case of a single micro-strip line, but still not negligible

Magnitude of reflection coefficient $|S_{11dd}|$ as a function of the Slot Length

Cut-outs in plane 10 mil along the differential micro-strip line and 80 mil across the line may cause SI problems at 10 Gbps



Strip line configuration to investigate effect of slot in the closest plane layer "Plane1"

- Simple 6-layer stackup
- Wideband Debye dispersion and loss models used for the dielectrics
- 6-mil wide strip line segment in the inner layer "Signal3"

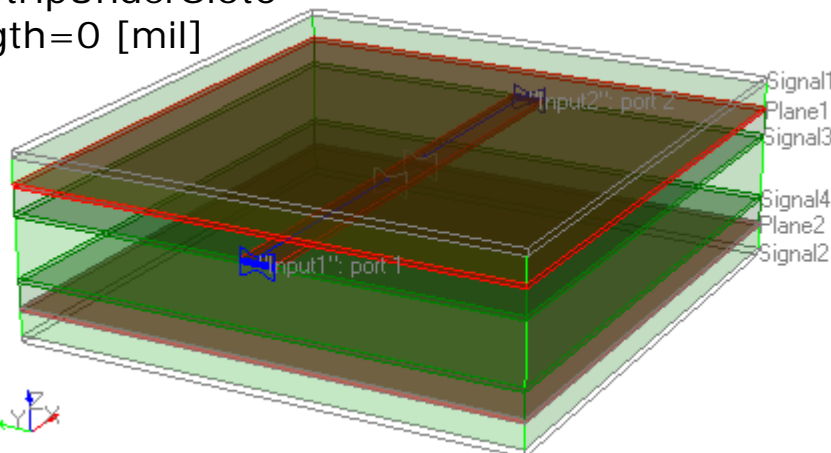
Materials and stackup in Simbeor Solution

Solution: "CrossingSplit2"

Project1

- Materials
 - "Copper", RR=1
 - "FR4", Dk=4.1, LT=0.02, PLM=WD
 - "Vacuum"
 - "prepreg", Dk=4.2, LT=0.02, PLM=WD
- StackUp: LU=[mil], NL=11, T=31.48
 - 1| Signal: "Signal1", T=1.2, Ins="Vacuum"
 - 2| Medium: T=4, Ins="FR4"
 - 3| Plane: "Plane1", Mat="Copper", T=0.77, Ins="FR4"
 - 4| Medium: T=4, Ins="prepreg"
 - 5| Signal: "Signal3", T=0.77, Ins="prepreg"
 - 6| Medium: T=10, Ins="FR4"
 - 7| Signal: "Signal4", T=0.77, Ins="prepreg"
 - 8| Medium: T=4, Ins="prepreg"
 - 9| Plane: "Plane2", Mat="Copper", T=0.77, Ins="FR4"
 - 10| Medium: T=4, Ins="FR4"
 - 11| Signal: "Signal2", T=1.2, Ins="Vacuum"

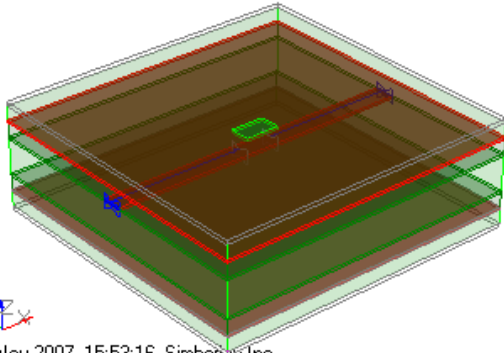
Circuit StripUnderSlot0
SlotLength=0 [mil]



17 Nov 2007, 15:45:02, Simberian Inc.

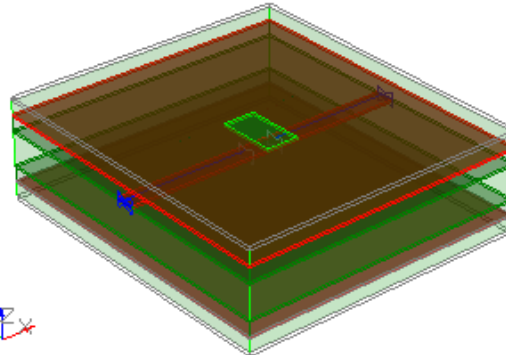
5 circuits with different slot length and with slot width 10 mil (size along the t-line)

Circuit StripUnderSlot1
SlotLength=6 [mil]



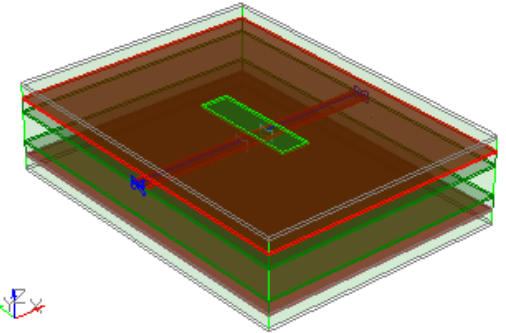
17 Nov 2007, 15:53:16, Simberian Inc.

Circuit StripUnderSlot2
SlotLength=18 [mil]



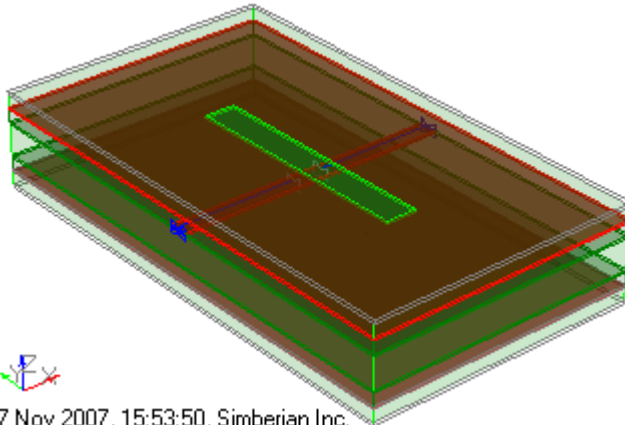
17 Nov 2007, 15:53:28, Simberian Inc.

Circuit StripUnderSlot3
SlotLength=39 [mil]



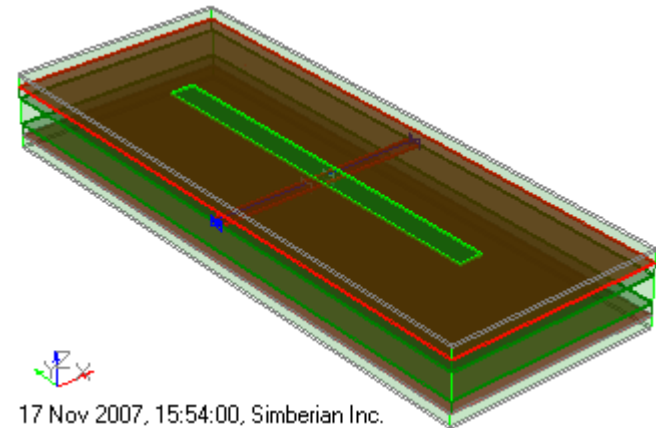
17 Nov 2007, 15:53:38, Simberian Inc.

Circuit StripUnderSlot4
SlotLength=78 [mil]



17 Nov 2007, 15:53:50, Simberian Inc.

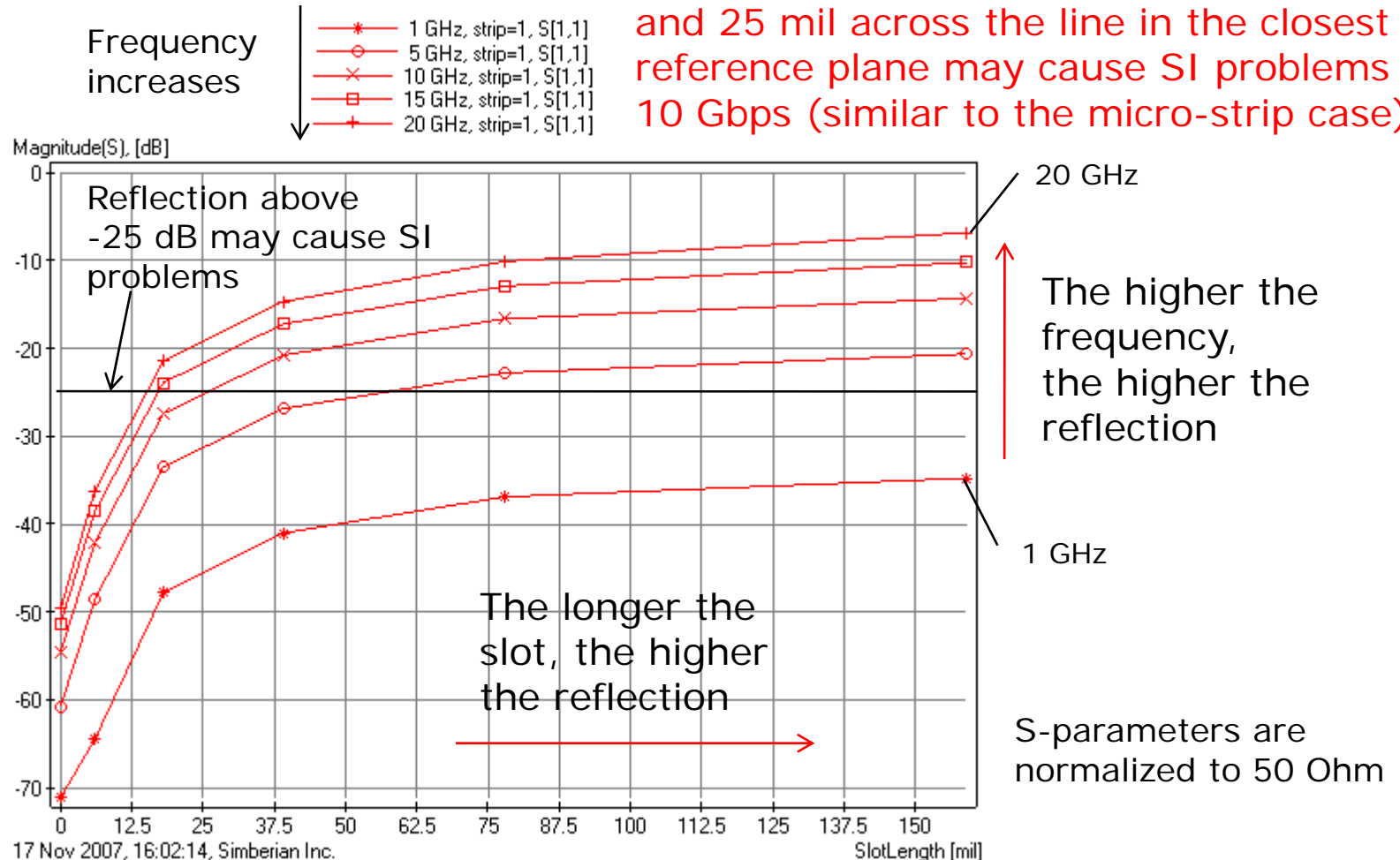
Circuit StripUnderSlot5
SlotLength=159 [mil]



17 Nov 2007, 15:54:00, Simberian Inc.

Magnitude of reflection coefficient |S11| as a function of the Slot Length

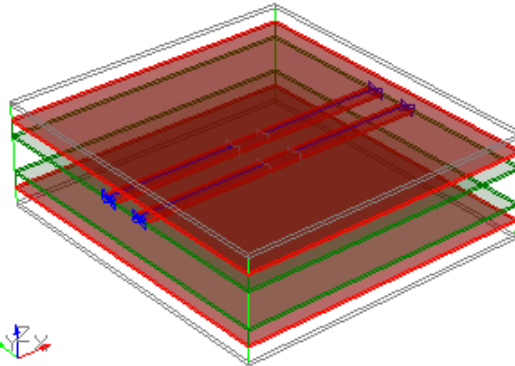
Cut-outs 10 mil along the single strip line and 25 mil across the line in the closest reference plane may cause SI problems at 10 Gbps (similar to the micro-strip case)



5 circuits describing differential strip-lines with a slot in the closest plane layer

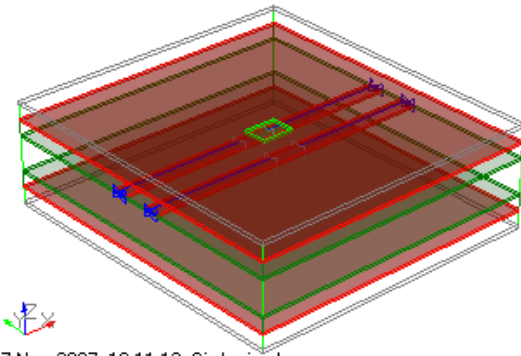
Two 5-mil wide strips in the layer "Signal3", 12.5 mil apart (about 100 Ohm differential impedance)

Circuit DStripUnderSlot0
SlotLength=0 [mil]



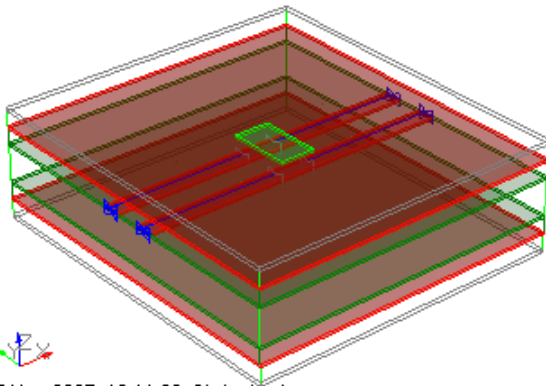
17 Nov 2007, 16:10:57, Simberian Inc.

Circuit DStripUnderSlot1
SlotLength=7.5 [mil]



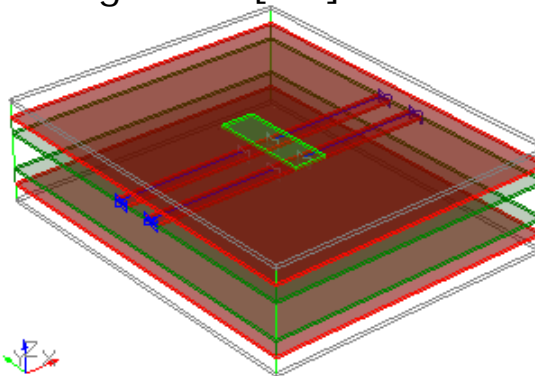
17 Nov 2007, 16:11:12, Simberian Inc.

Circuit DStripUnderSlot2
SlotLength=17.5 [mil]



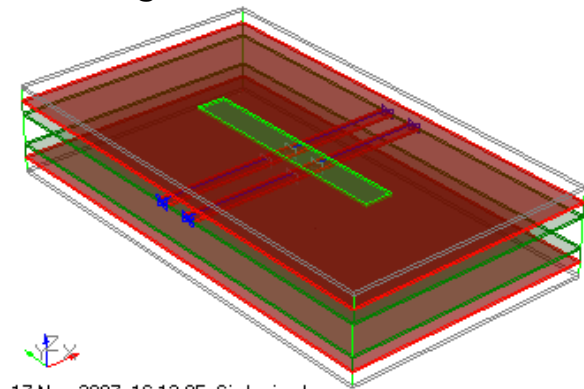
17 Nov 2007, 16:11:26, Simberian Inc.

Circuit DStripUnderSlot3
SlotLength=30 [mil]



17 Nov 2007, 16:11:51, Simberian Inc.

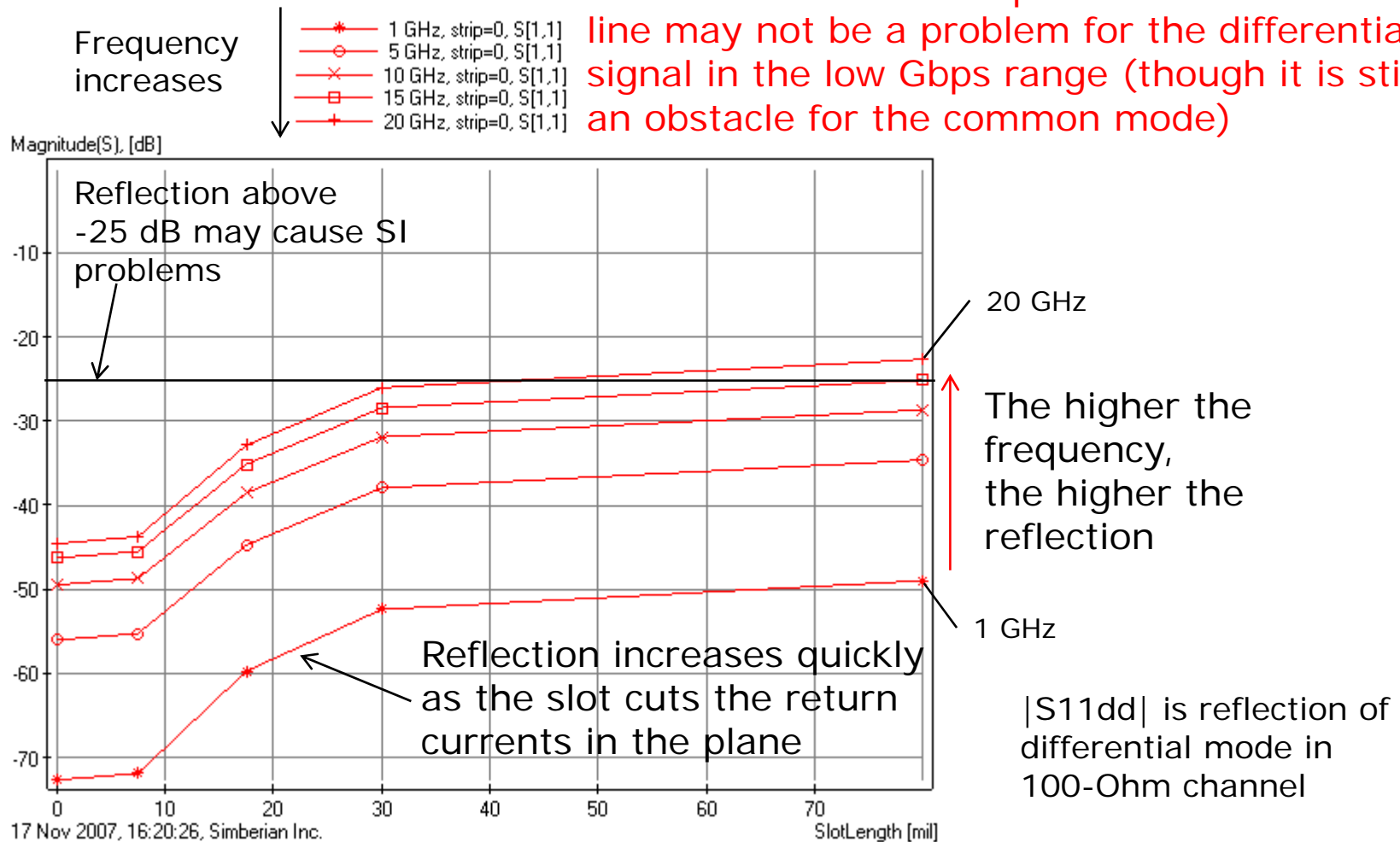
Circuit DStripUnderSlot4
SlotLength=80 [mil]



17 Nov 2007, 16:12:05, Simberian Inc.

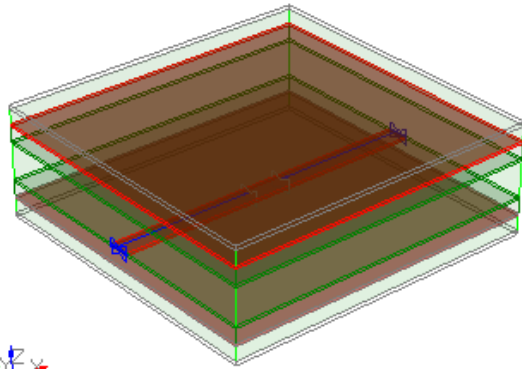
Magnitude of reflection coefficient $|S_{11dd}|$ as a function of the Slot Length

Cut-outs in the closest plane of differential strip line may not be a problem for the differential signal in the low Gbps range (though it is still an obstacle for the common mode)



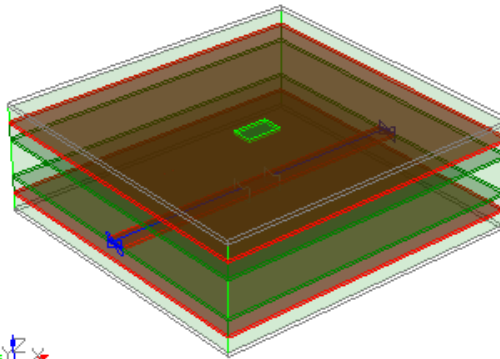
6 circuits with strip in layer "Signal4" and cut-outs in the remote plane layer "Plane1"

Circuit StripUnderSlot1
SlotLength=0 [mil]



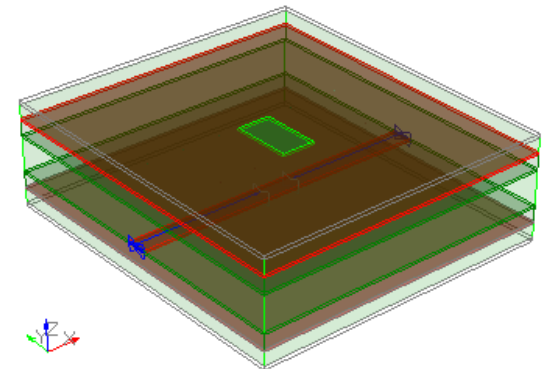
17 Nov 2007, 16:37:58, Simberian Inc.

Circuit StripUnderSlot1
SlotLength=6 [mil]



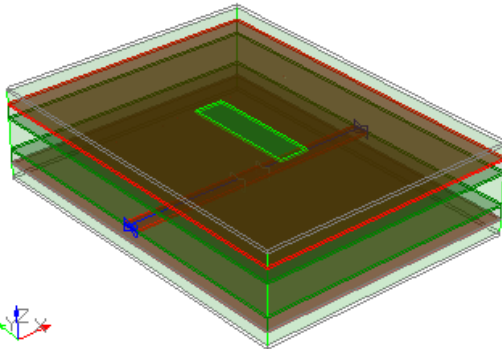
17 Nov 2007, 16:38:12, Simberian Inc.

Circuit StripUnderSlot2
SlotLength=18 [mil]



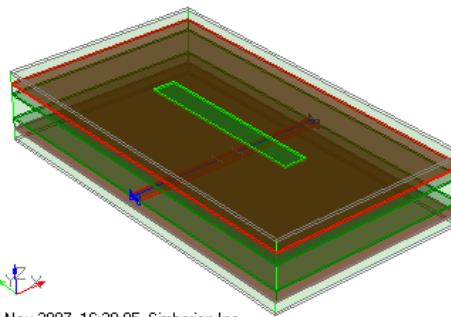
17 Nov 2007, 16:38:36, Simberian Inc.

Circuit StripUnderSlot3
SlotLength=39 [mil]



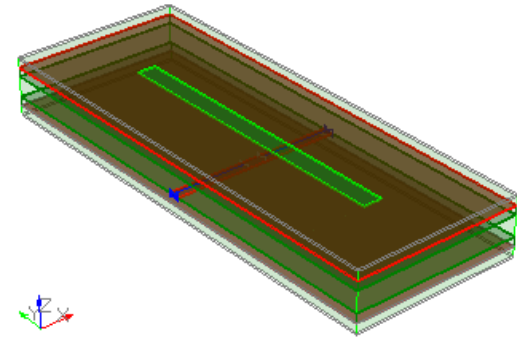
17 Nov 2007, 16:38:49, Simberian Inc.

Circuit StripUnderSlot4
SlotLength=78 [mil]



17 Nov 2007, 16:39:05, Simberian Inc.

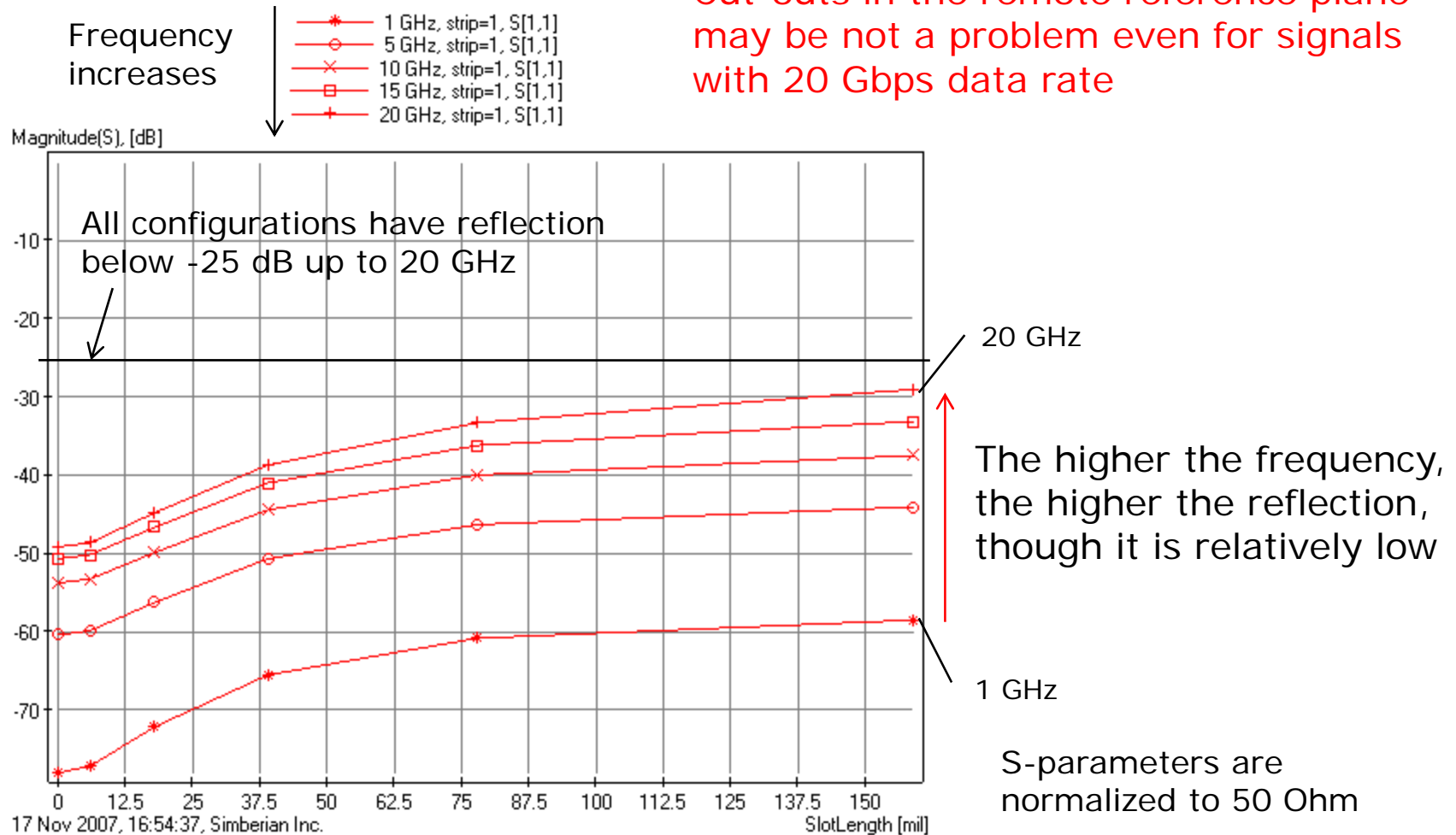
Circuit StripUnderSlot5
SlotLength=159 [mil]



17 Nov 2007, 16:39:27, Simberian Inc.

Magnitude of reflection coefficient $|S_{11}|$ as a function of the Slot Length

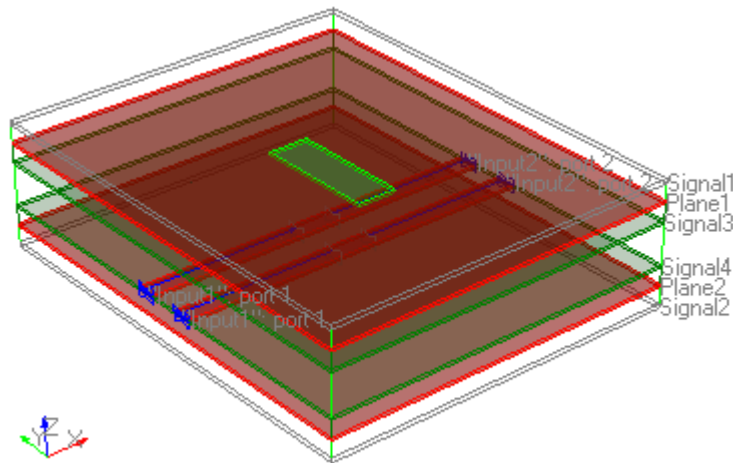
Cut-outs in the remote reference plane may be not a problem even for signals with 20 Gbps data rate



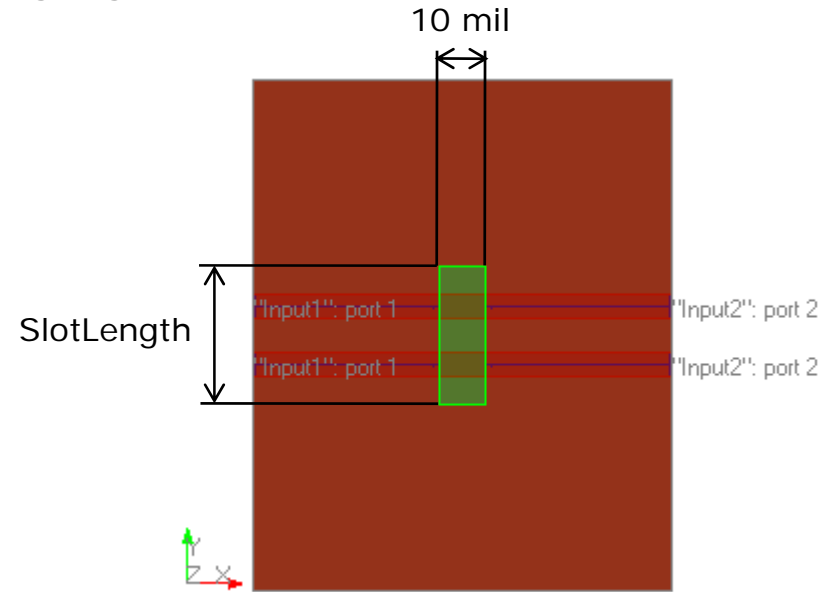
Differential strips in layer "Signal4" and slots in the remote plane layer "Plane2"

Two 5-mil wide strips in the layer "Signal4", 12.5 mil apart (about 100 Ohm differential impedance)

SlotLength is a parameter changing from 0 to 80 mil

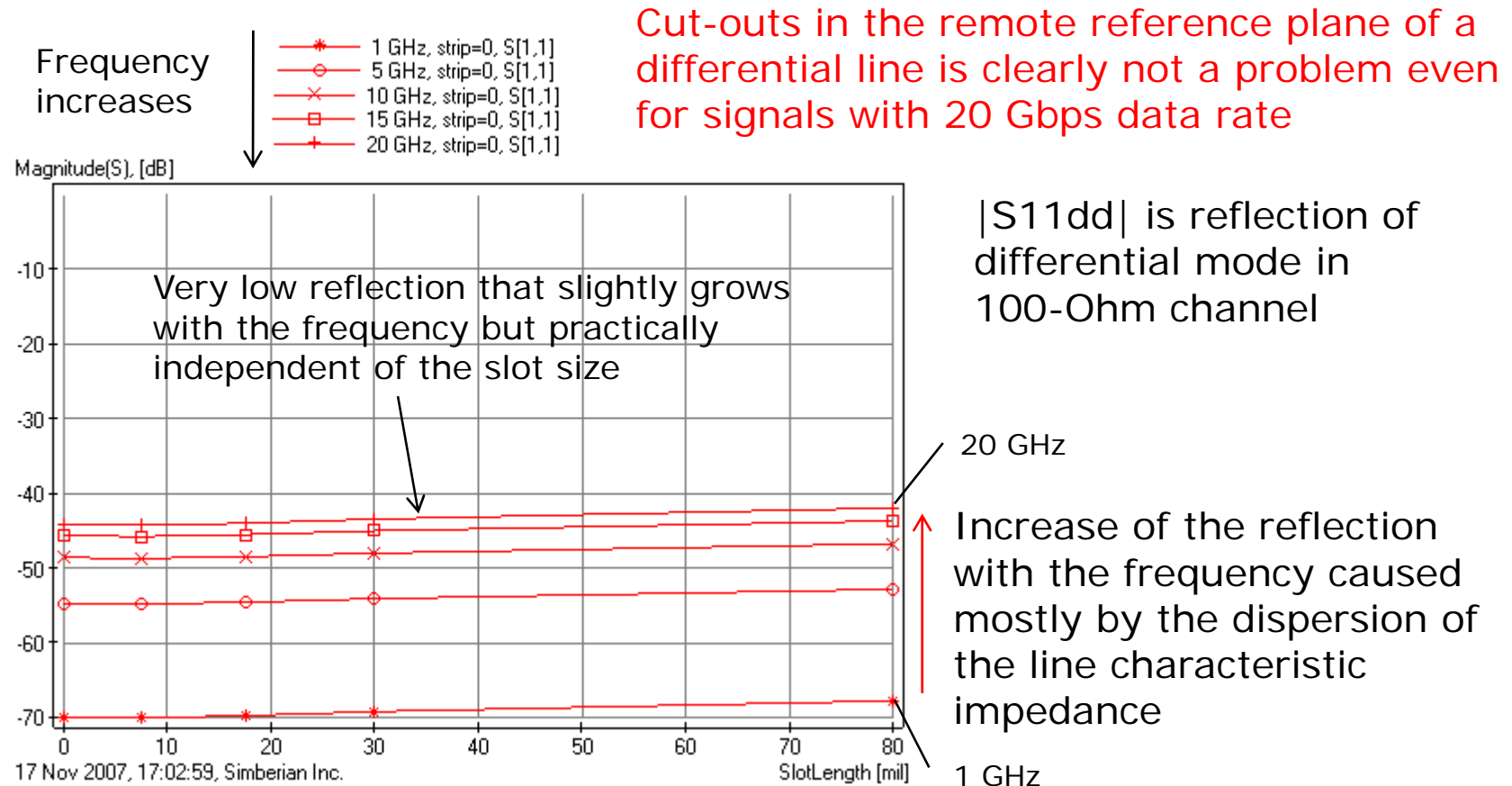


18 Nov 2007, 08:44:36, Simberian Inc.



17 Nov 2007, 17:01:09, Simberian Inc.

Magnitude of reflection coefficient $|S_{11dd}|$ as a function of the Slot Length



How to use these results?

- ❑ Such numerical experiments can be used to plan positions of plane layers with cut-outs in a stack-up for a particular data rate and to generate rules for routing multi-gigabit nets for instance
- ❑ In case if cut-outs cannot be avoided, S-parameter models for localized cut-outs can be generated and used in a system-level solver
- ❑ Slot de-coupling or by-passing with capacitors can be also investigated with a full-wave solver
 - Such configuration may not reduce the reflection over a wide frequency band but may be helpful to reduce the radiation from the oversized slots (valid also for common mode in case of differential t-lines)

What about more complicated split-plane configurations?

- In case of moats or complicated plane splits the signal may be not just reflected but transmitted by the slot line across the board and either radiated or coupled to the other t-lines crossing the same slot
 - It may cause both cross-talk (SI) and radiation (EMI) problems
 - Complete electromagnetic analysis of such structures is rarely possible and not practical in many cases
 - Only hybrid de-compositional system-level analysis of such structures with strip, slot and parallel-plane models may predict the behavior (multiple components of a system have to be included into such analysis)
- Even if differential signal in differential pair is not affected by the slot, the common mode may be affected and either reflected or coupled to the slot-line and require either the system-level analysis or slot-line loading or termination preventing SI and EMI problems
- Decoupling capacitors can help to reduce the coupling to the slot and dump propagation of energy along the slots in complicated cut-outs, both in single line and common mode in differential line cases

Solutions and contact

- Solution files are available for download from the simberian web site
 - http://www.simberian.com/AppNotes/Solutions/SlotsInReferencePlanes_2007_09.zip
- Send questions and comments to
 - General: info@simberian.com
 - Sales: sales@simberian.com
 - Support: support@simberian.com
- Web site www.simberian.com