

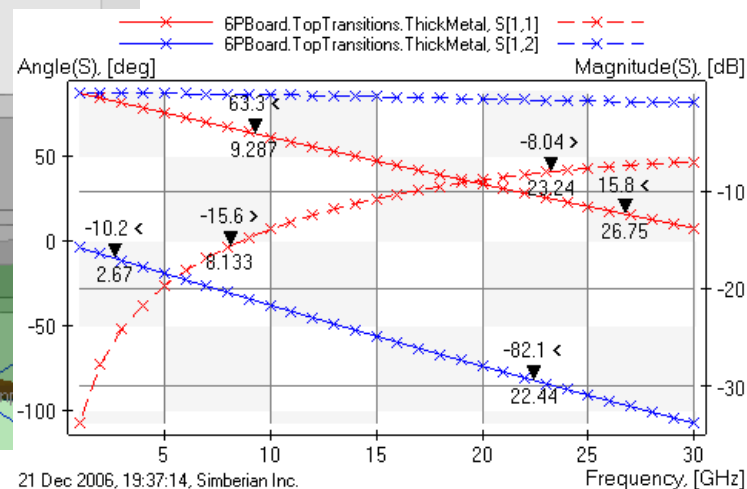
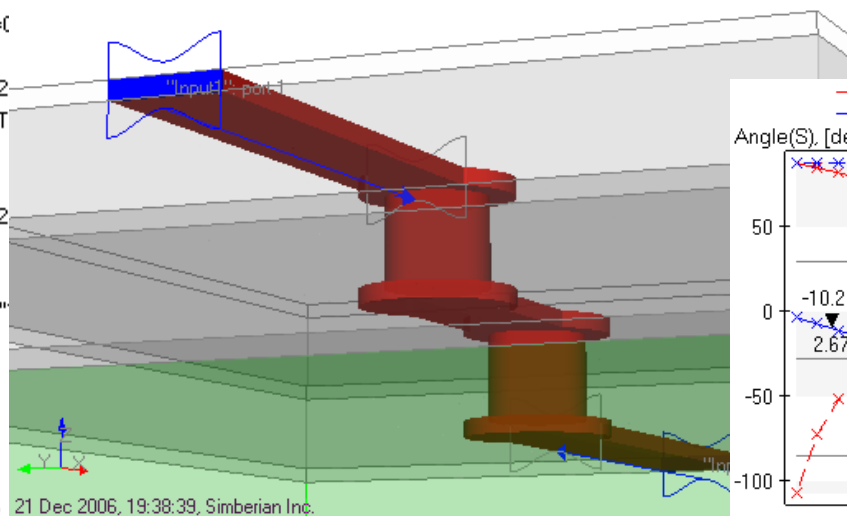
Electromagnetic Analysis of Spiral Inductors with Simbeor 2008

Solution: "MicroVias"

- 6PBoard
 - Materials
 - "copper", RRes=1, Rough=0.01
 - "IdealMetal"
 - "prepreg", DK=4.7, LT=C
 - "Vacuum"
 - "FR4", DK=4.2, LT=0.02
 - StackUp: LU=[mil], NL=15, T
 - TopTransitions
 - CircuitData: LU=[mil]
 - Multiport: 2 inputs, 2
 - LatticeBox
 - Geometry
 - GeoComposite: "
 - TLines
 - Inputs
 - ThickMetal
 - CollapsedMetal
 - BottomTransition
 - Graph1(MultiportParameters vs. 21 Dec 2006, 19:38:39, Simberian Inc.)
 - Graph2(MultiportParameters vs. Frequency)

Simberian, Inc.

www.simberian.com



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Overview

- Introduction
- Benchmark inductor
- Stacked inductors on silicon
- Conclusion

Introduction

- ❑ Planar inductors are commonly used in ICs, MICs, PCBs and in Packages (embedded inductors)
- ❑ They typically designed with quasi-static PEEC-type tools, but often require electromagnetic analysis to verify the system behavior over wide frequency band and to take into account effects that cannot be captured by a quasi-static analysis
- ❑ Some examples of analysis of planar and stacked inductors with Simbeor solver are provided here
- ❑ Simbeor 2008 built on August 25th is used to generate all examples

Benchmark inductor

- ❑ **Oversized spiral inductor** introduced first by M. Rittweger and I. Wolff at MTT-S in 1990 and investigated experimentally and by different methods in multiple papers

IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 40, NO. 12, DECEMBER 1992

2219

Analysis of 3-D Metallization Structures by a Full-Wave Spectral Domain Technique

Thomas Becks, *Member, IEEE* and Ingo Wolff, *Fellow, IEEE*

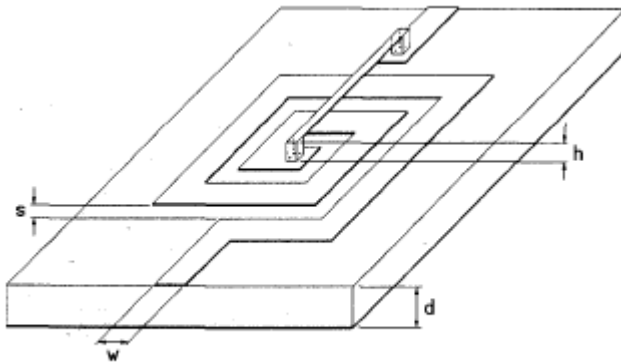


Fig. 1. Schematic view on a rectangular spiral inductor in microstrip technique.

Good test to distinguish quasi-static from full-wave solution!

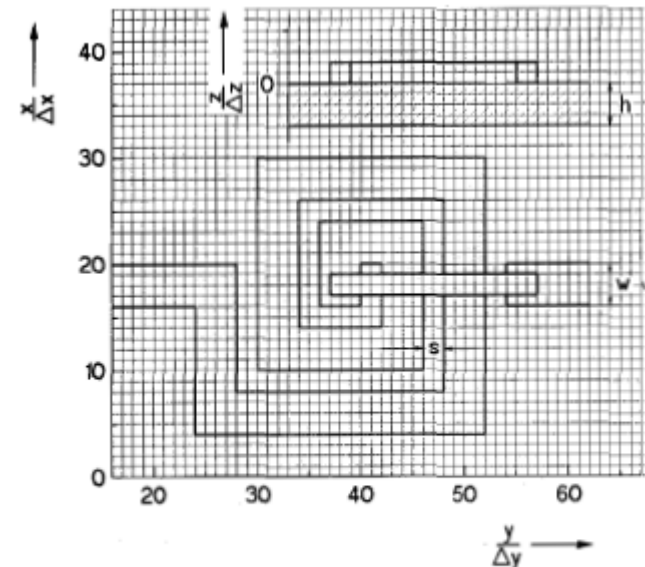
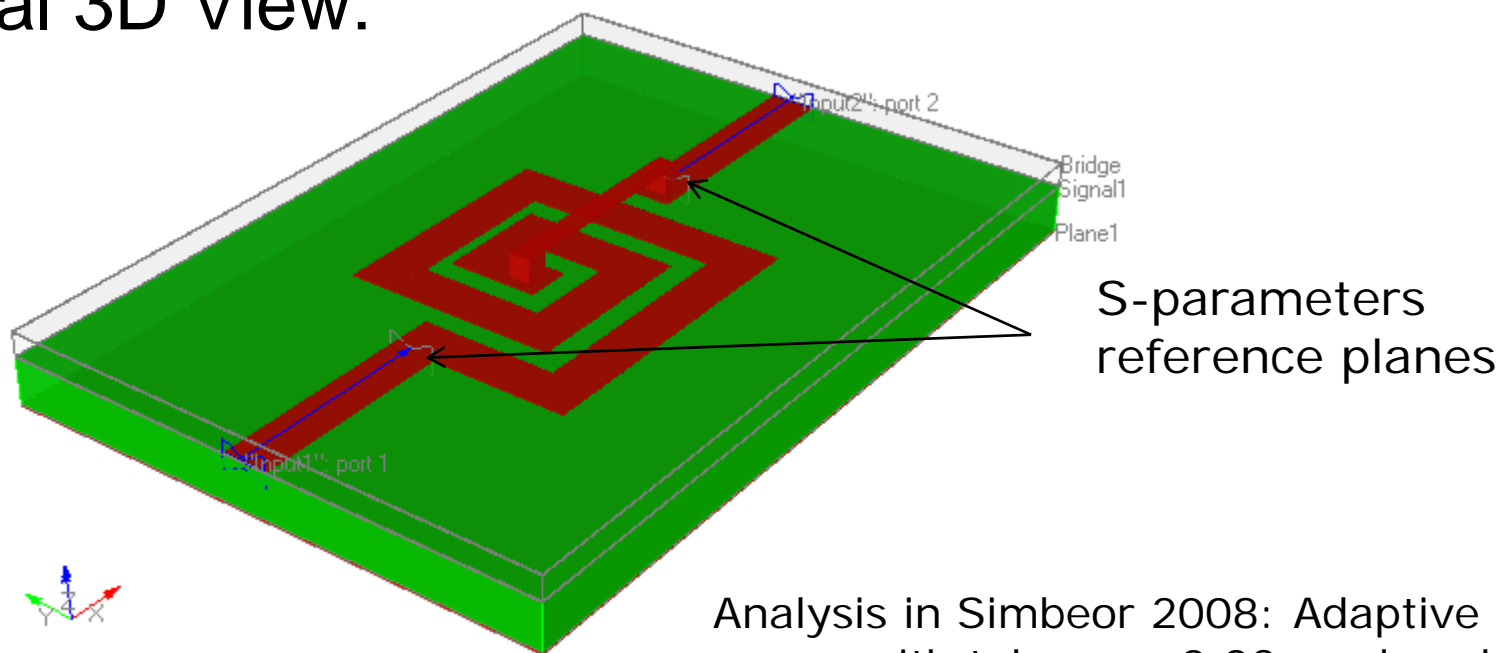


Fig. 11. Layout of the rectangular spiral inductor $\epsilon_r = 9.8$, $d = 635 \mu\text{m}$, $w = 625 \mu\text{m}$, $s = 312.5 \mu\text{m}$, $h = 317.5 \mu\text{m}$, $\Delta x = \Delta y = 156.25 \mu\text{m}$, and $\Delta z = 158.75 \mu\text{m}$.

Benchmark inductor problem settings

- Draw in the Editor with 10 rectangles, 2 cuboids and 2 segments of TLine with attached inputs
- Final 3D View:

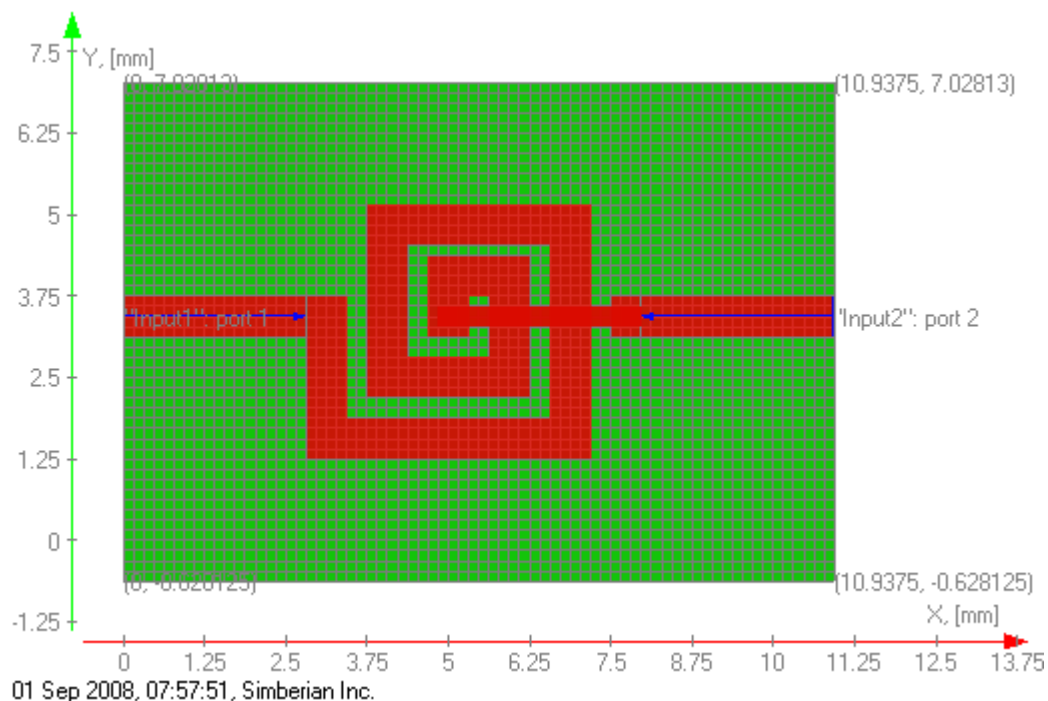
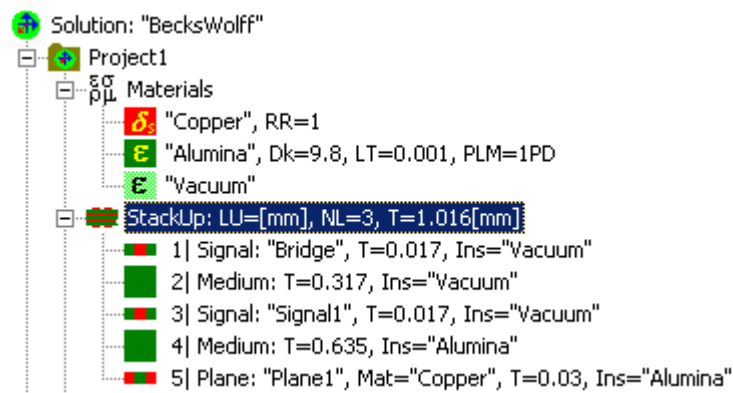


01 Sep 2008, 07:56:58, Simberian Inc.

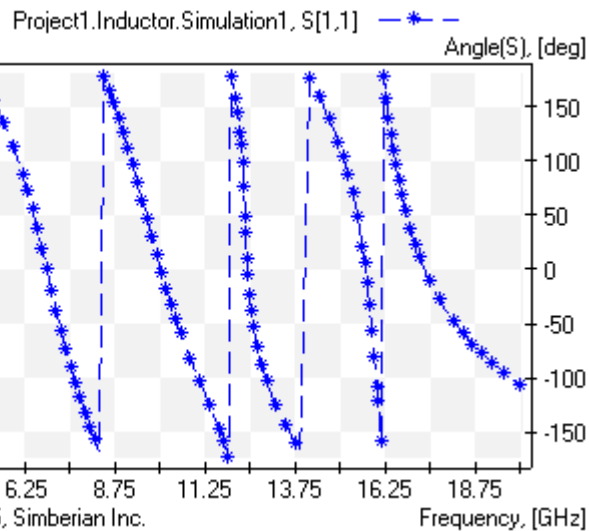
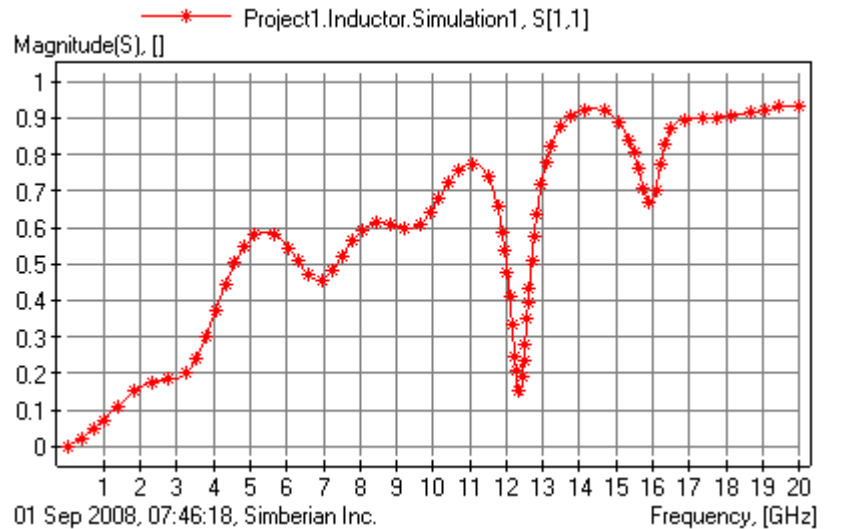
Analysis in Simbeor 2008: Adaptive sweep with tolerance 0.02 produced 218 frequency points in 40 min

Benchmark inductor problem settings

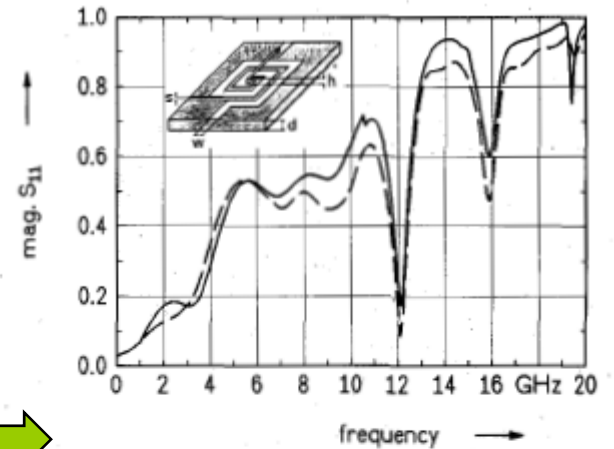
- Metal type and thickness, dielectric loss tangent are guessed:
 - 1/2 Oz copper, DK=9.8, LT=0.001 at 10 GHz, 1-pole Debye with $F_r=1$ THz



Benchmark inductor: S[1,1]



Good correspondence



Becks&Wolff, © IEEE

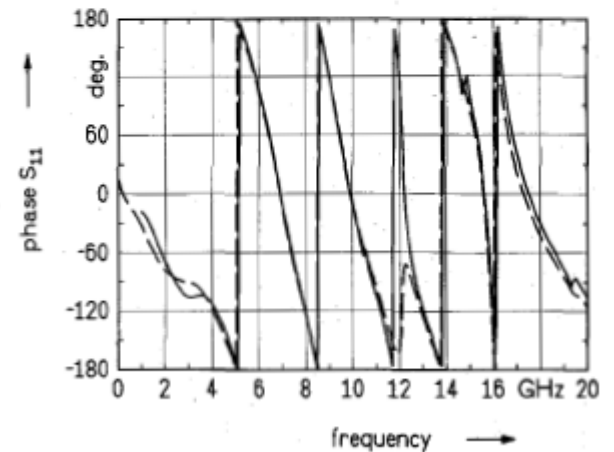
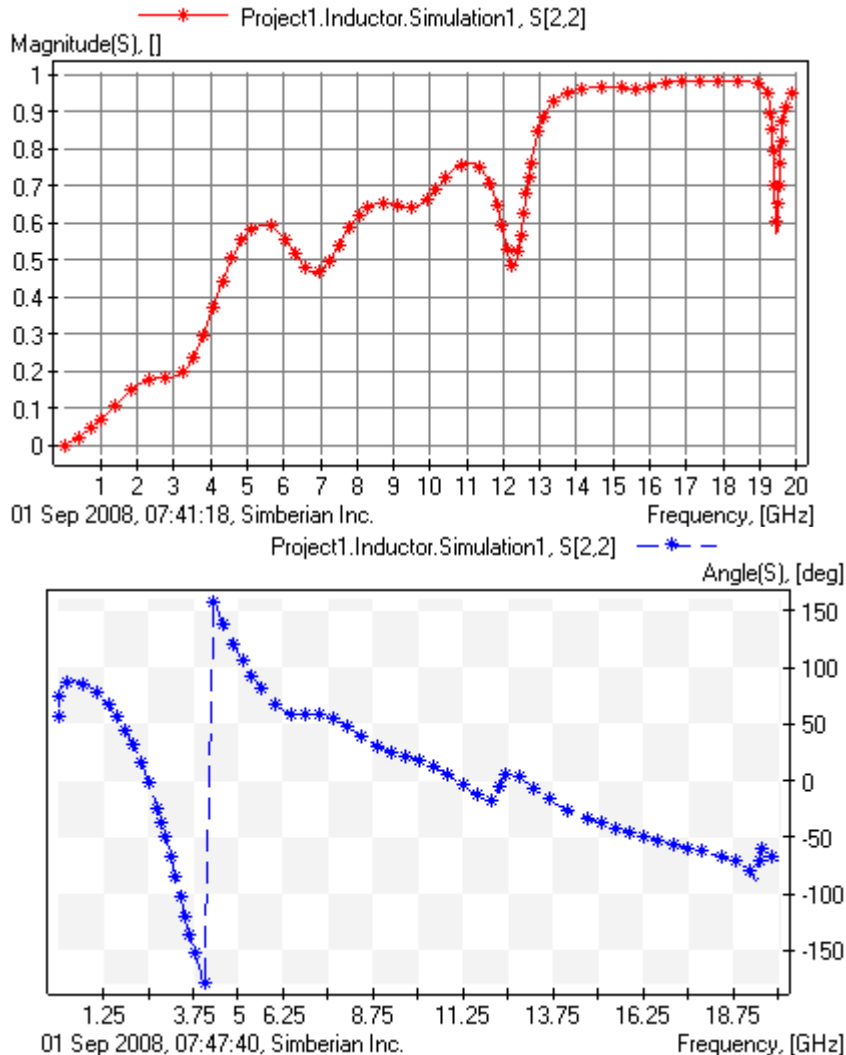


Fig. 12. Reflection coefficient S_{11} of the structure shown in Fig. 11. (—) calculated, (---) measured. Top: Magnitude of S_{11} . Bottom: Phase of S_{11} .

Benchmark inductor: S[2,2]



Good correspondence



Becks&Wolff, © IEEE

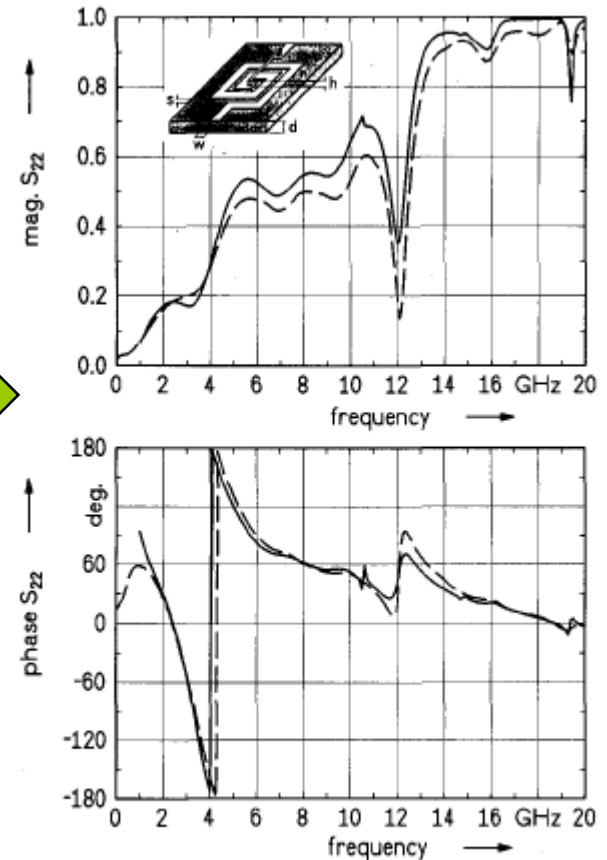
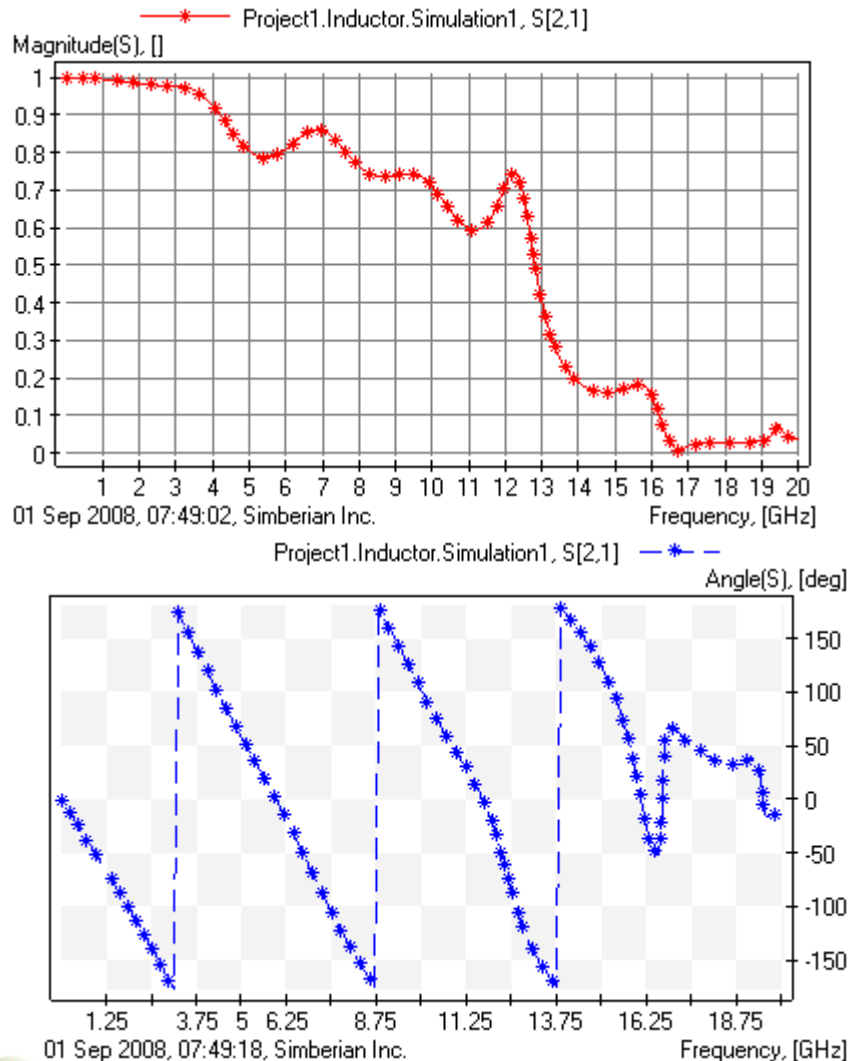


Fig. 13. Reflection coefficient S_{22} of the structure shown in Fig. 11. (—) calculated, (---) measured. Top: Magnitude of S_{22} . Bottom: Phase of S_{22} .

Benchmark inductor: S[2,1]



Good correspondence



Becks&Wolff, © IEEE

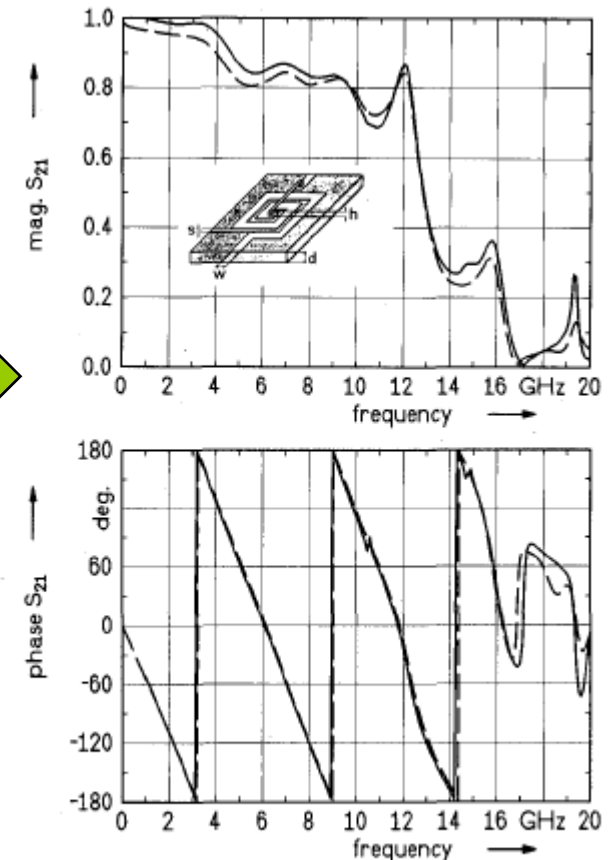


Fig. 14. Transmission coefficient S_{21} of the structure shown in Fig. 11. (—) calculated, (---) measured. Top: Magnitude of S_{21} . Bottom: Phase of S_{21} .

Stacked miniature inductors

- W.Y. Yin at al. Vertical topologies of miniature multi-spiral stacked inductors, IEEE Trans. on MTT, v. 56, N2, 2008, p. 475-484.

CMOS 0.18 μm process, $D=40 \mu\text{m}$, $W=5 \mu\text{m}$, $S=2.5 \mu\text{m}$
 Thicknesses of metal and dielectric layers are not provided
 We investigate just the idea with Simbeor 2008

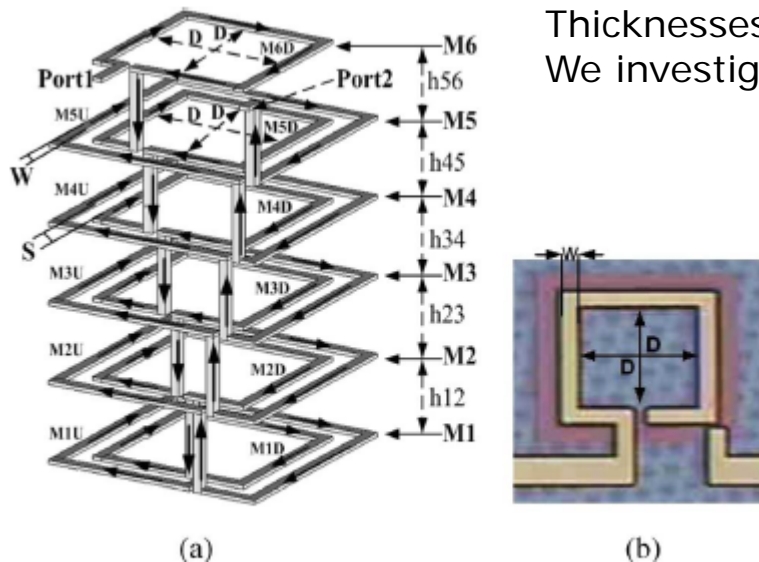
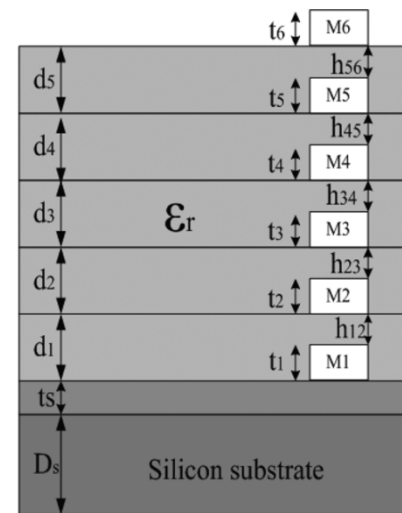
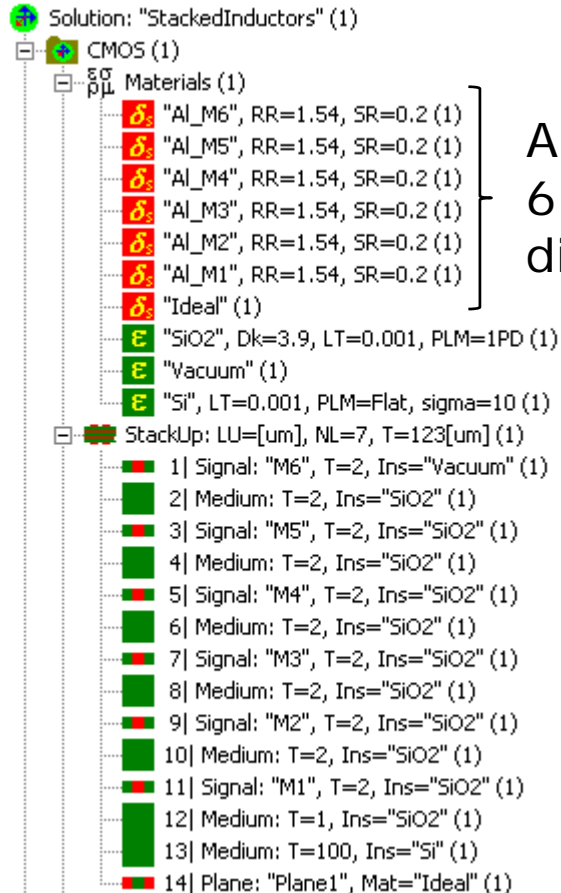


Fig. 1. (a) Vertical topology of a square six-spiral stacked inductor. (b) Its on-chip top view.



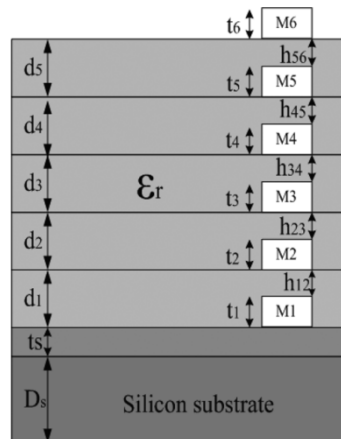
Materials and stackup in Simbeor



Aluminum is used as conductor
6 identical conductors created to use different color for different layers

All insulator layer are simulated as SiO2, with DK=3.9, LT=0.001 at 10 GHz as 1-pole Debye model

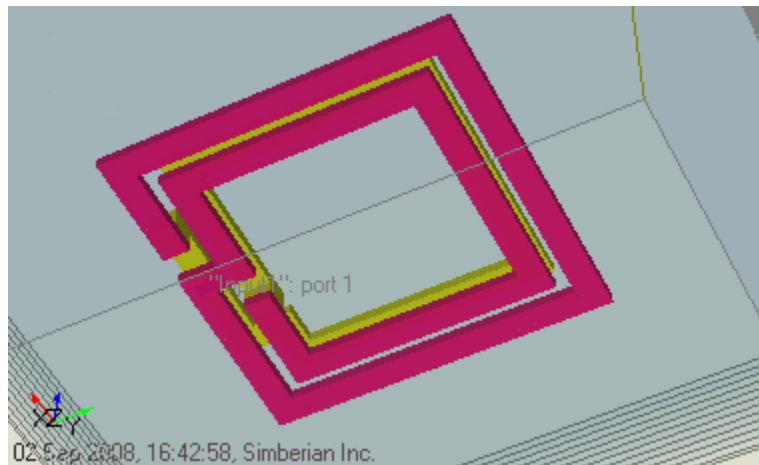
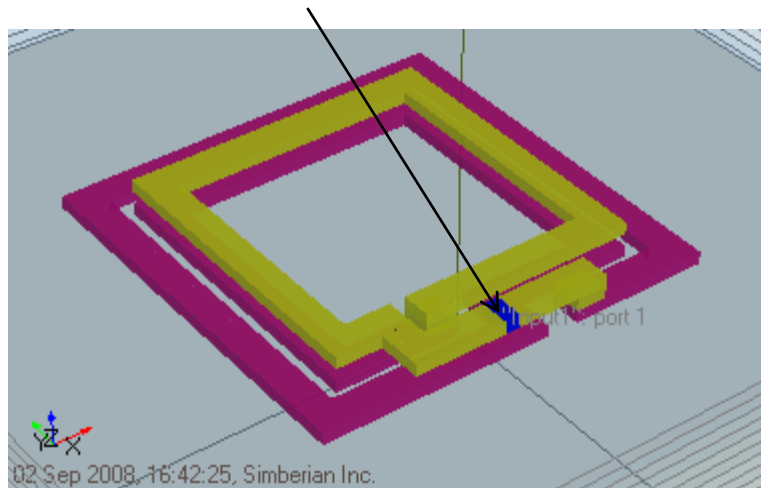
Silicon simulated as insulator with conductivity 10 Sm/m or resistivity 0.1 Ohm-m (lightly doped)



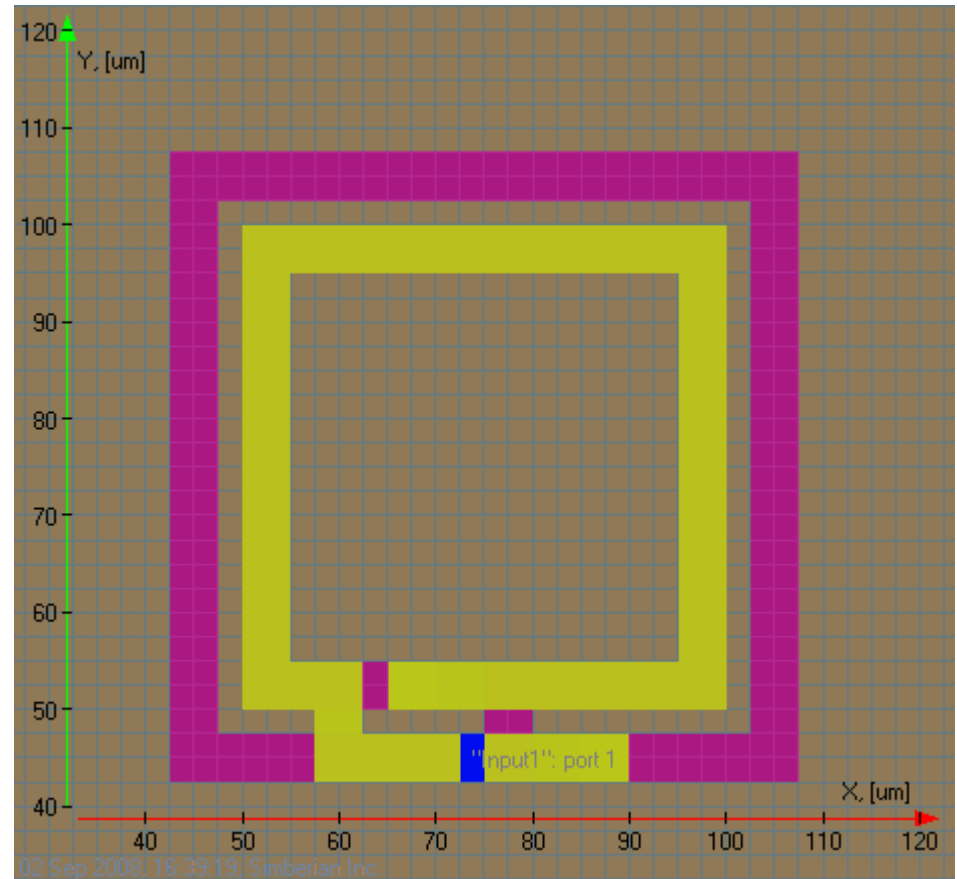
All t1-t6 are 2 um, d1-d5 are 4 um, t_s=1 um, D_s=100 um

Two-level inductor (M1-M2)

Lumped port to measure inductance

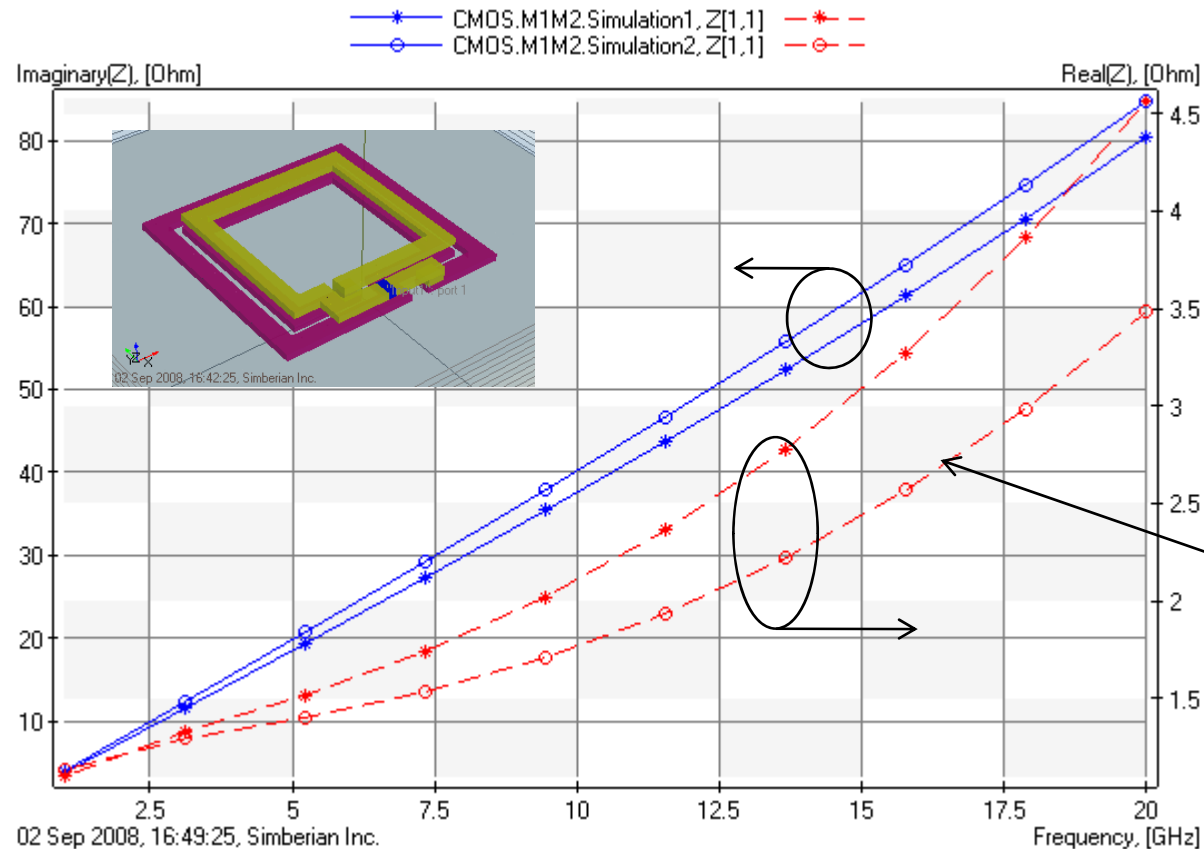


Only rectangles and two cuboids (vias) are used to draw the inductor, cell size 2.5 μm



Two-level inductor (M1-M2)

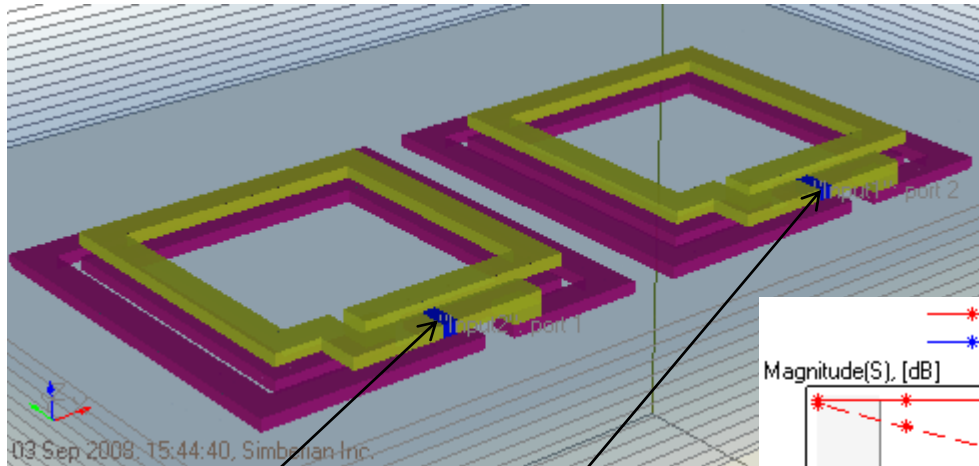
- Simulated with thick metal (stars) and with collapsed metal (circles)
- Inductance is 0.6 nH with thick metal and 0.64 nH with collapsed



Losses are under-estimated with collapsed metal (2.5D model)

Coupled two-level inductors (M1-M2)

- Substrate coupling can be investigated

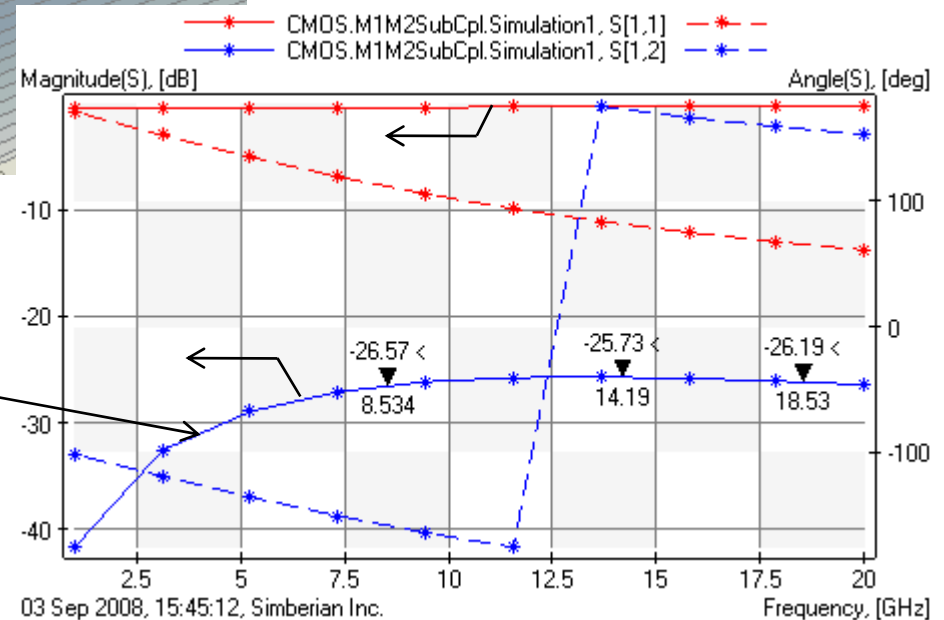


Port 1

Port 2

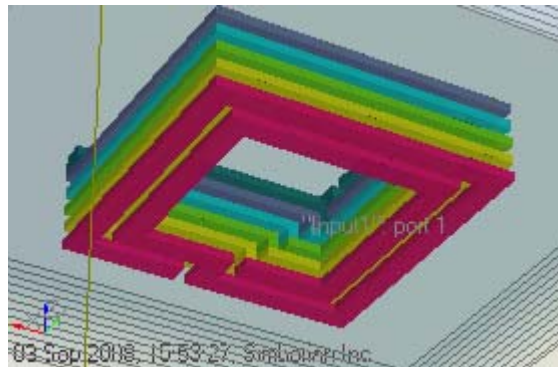
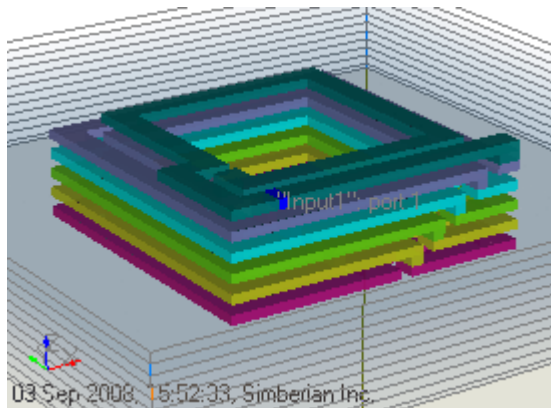
Transmission from port 2 to port 1

50-Ohm normalized S-parameters

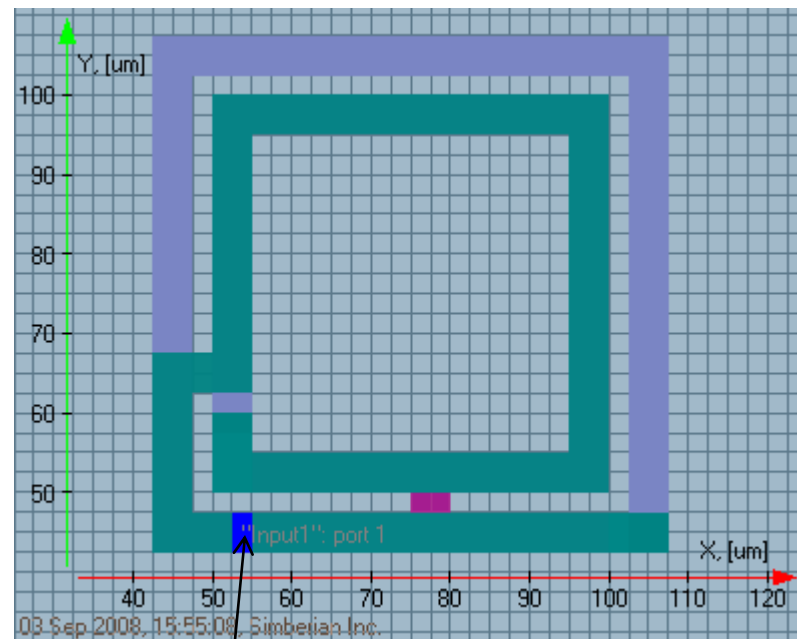


Six-level inductor

- The same principle of repetitive loops as in the case of two level



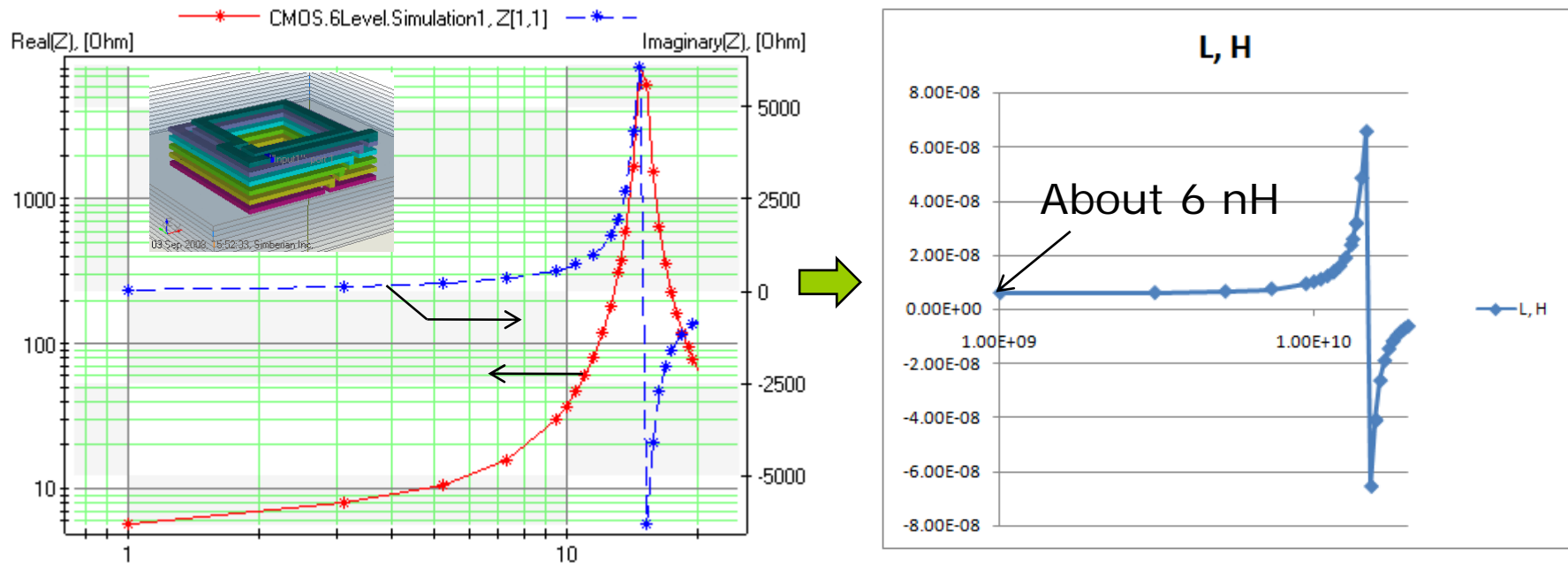
Only rectangles and cuboids used to draw the inductor, cell size 2.5 μm



Lumped port to measure the inductance

Six-level inductor

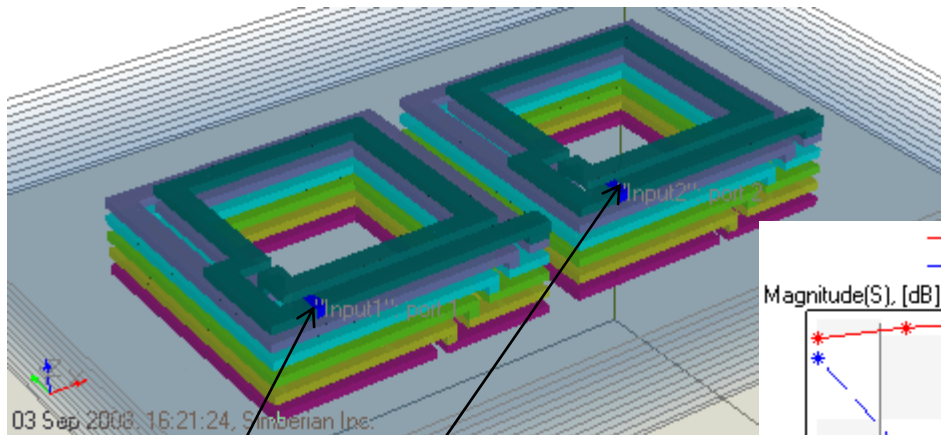
- Full-wave analysis captures inductance at low frequency and self-resonance of the inductor taking into account skin-effect both in conductors and in silicon



Z-parameters are exported from Simbeor into CSV-file to calculate and to plot the inductance

Coupled six-level inductors

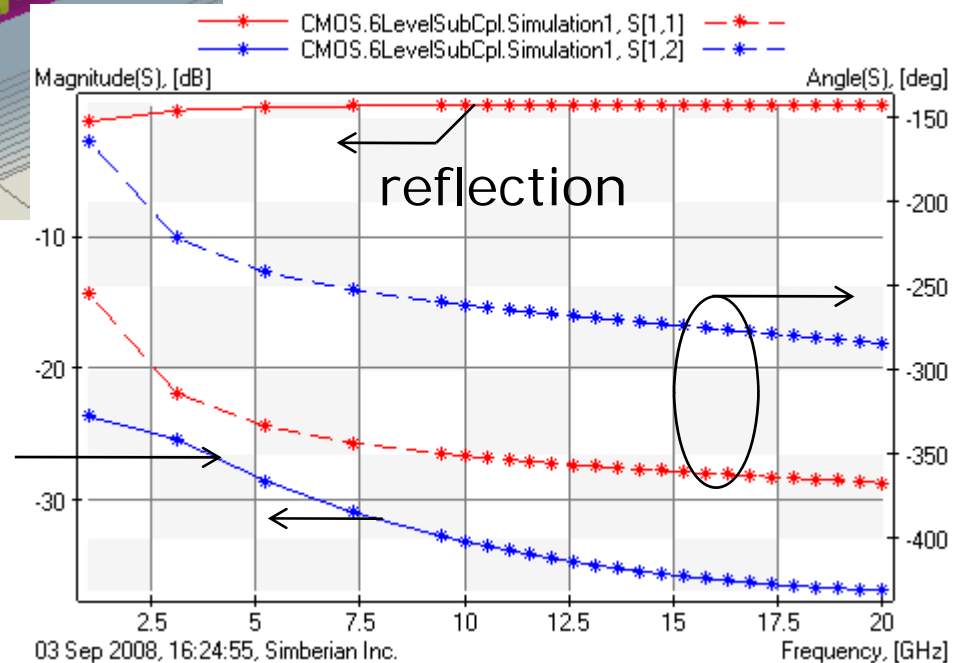
- Created by copying and shifting inductor in the editor
- Takes about 4 hours to extract 30 frequency points



Port 1 Port 2

Transmission from
port 2 to port 1

50-Ohm normalized
S-parameters



Conclusion

- ❑ Simbeor provides possibility to extract parameters of some types of inductors over wide frequency band both for PCB/package and IC levels
- ❑ Analysis includes low-frequency effects related to substrate coupling, transition to skin-effect and skin-effect both in conductors and in silicon substrate
- ❑ Analysis also includes dielectric dispersion and loss (affects self-resonance and coupling)
- ❑ Simbeor may be used as complimentary to PEEC inductance design tools to verify the high-frequency behavior or substrate coupling or to investigate “what if” scenarios
- ❑ Only manual description of geometry is available so far and analysis is relatively slow
 - Analysis can be accelerated by reducing the maximal critical frequency – it was 20 and 10 GHz in the provided examples
 - Analysis may be considerably slower on circular or octagonal shapes – Simbeor’s super-grid is not optimized for such structures

Solutions and contact

- Simbeor solution files are available for download from the simberian web site
 - http://www.simberian.com/AppNotes/Solutions/Inductors_2008_03.zip
- Send questions and comments to
 - General: info@simberian.com
 - Sales: sales@simberian.com
 - Support: support@simberian.com
- Web site www.simberian.com