

Designing localizable minimal-reflection via-holes for multi-gigabit interconnects

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Abstract

Via-hole transitions are the major contributors to signal degradation in PCB and packaging interconnects. Signal reflection, coupling to parallel-planes, radiation, and resonances in interconnects with via-holes may destroy the signal in such a way that it becomes impossible to restore it with any type of pre-emphasis and equalization. Design of controlled-impedance via-holes with the minimal reflection is especially important task for interconnects with data rates 6 Gb/s and higher with the signal spectrum in the microwave frequency band. This paper shows how to approach the via-hole modeling problem and provides brief overview of different via-hole types and via-hole analysis techniques usable for design of multi-gigabit data channels. Practical examples of via-hole design with experimental validation are provided.

Introduction

Via-holes are structures connecting components and traces in different layers of multi-layered printed circuit boards (PCBs) or packages. They are relatively small comparing to the traces and behave almost like ideal connections at low frequencies due to small electrical length and small impedance of the current return path (**see Glossary for definition of some terms used here**). Because of that, the via-holes were either completely ignored in the analysis or simulated with a lumped inductance and/or with a lumped capacitance, calculated with approximate equations. All this was working fine until recently, when the spectrum of the signals transmitted through the interconnects reached the microwave range (above 3 GHz for 6 Gb/s signals). The via-holes behave as distributed structures at these frequencies and must be simulated as the distributed structures. Unfortunately, not all vias are identical from the analysis point of view and some classification of different vias may be helpful before even approaching the analysis. **Some via-holes can be simulated in isolation from the rest of the board and some may require the analysis of the whole board with all reference and power distribution structures included.** The vias from first group can be termed as localizable and this paper explains how to distinguish and to design such vias.

Current return path and localizability

Via-holes are often classified by the span in a board stack-up as through, buried, blind or back-drilled and so on. Via-hole current return path localization may be used to separate all those vias in two groups for analysis purpose. **Via-holes with the current return path in a small area around a via can be called localizable. Otherwise, if the current return path is spread over the board, the via can be called non-localizable.** Via-holes that connect traces with the same reference planes can be always analyzed in isolation (though they may radiate). It is not the case for the vias connecting traces with different reference planes (via-holes crossing one or more reference planes). Let's investigate the return current localization separately for **single-ended and differential via-holes**. Three different cases of the current return path for **single-ended vias** are shown in Fig. 1. They can be defined as follows:

- a) Planes are not connected or terminated and the return current is the "displacement" current between the planes - the problem is non-localizable for broadband analysis (Fig 1a) and requires analysis of the whole board.

- b) Planes are terminated with the decoupling capacitors and the return current is a combination of the “displacement” currents through capacitors and planes (Fig 1b) - capacitors have low impedance only in a narrow frequency band. Thus, the problem again is non-localizable for broadband EM analysis.
- c) Stitching vias are used to connect the reference planes for the connected layers and the return current is mostly conductive (Fig 1c) - problem can be localized (localizable) and solved with any boundary conditions (though the frequency band may be limited).

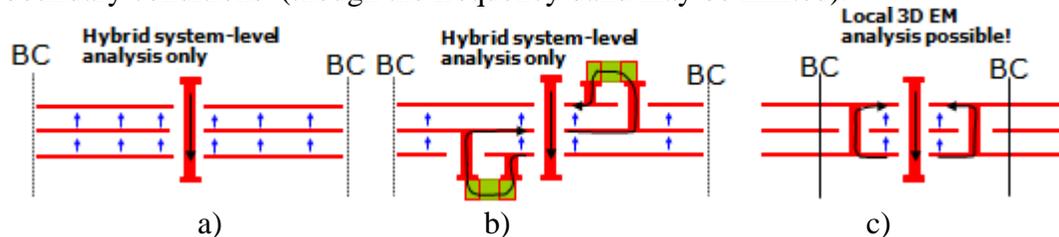


Fig. 1. Three types of the current return path localization for single-ended via-hole. Blue arrows show “displacement” current. BC – lines for possible boundaries for analysis.

For multi-gigabit signals single-ended vias always require electrically close stitching via-holes connecting all reference conductors of the connected transmission lines. Similar to a short-circuit condition in a t-lines that becomes an open circuit if t-line segment length is equal to quarter of wave-length, the stitching via-holes at a quarter wavelength distance (3.75 mm or 147 mil for 10 GHz for instance) do not provide the path for the return current and the structure becomes non-localizable. For practically purpose, localizability property of a via-hole can be estimated by investigation of S-parameters dependency either on the boundary conditions and simulation area in an electromagnetic simulator or on the geometry and size of a board in experiment. **Localizable via-holes are relatively independent of the simulation area or board shape and size and can be simulated in the isolation from the rest of the board and reliably reused as a design component.** Note that all reference planes of the connected transmission lines have to be connected by the stitching vias – otherwise the structure is not localizable by design. Not-localizable cases are usually difficult to simulate with a 3D full-wave analysis and parallel-plane (transmission plane) models may be used at lower frequencies and hybrid models may be required at higher frequencies. **The number of stitching via-holes to keep the localization may be up to 4-6 stitching vias or more per signal via for localization up to 20 GHz on a typical PCB.**

Differential vias are two-via transition through multiple parallel planes with possible stitching vias nearby. Two excitation modes can be defined for a symmetrical pair: differential and common (similar to differential t-lines). Differential mode has identical currents in both barrels flowing in the opposite direction. Common mode has two identical currents in the same direction. Signal in differential pair always contains differential mode (useful) and may contain common mode induced by asymmetries in driver and by discontinuities. **If two barrels are electrically close to each other, the differential mode is localizable and can be simulated with any boundary conditions at a sufficient distance as shown in Fig. 2a).** The common mode behavior is similar to the single-ended via and is not localizable without stitching vias nearby. Electrically close stitching vias may be used to confine the common mode and to simulate the structure in isolation from the rest of the board as shown in Fig. 2b).

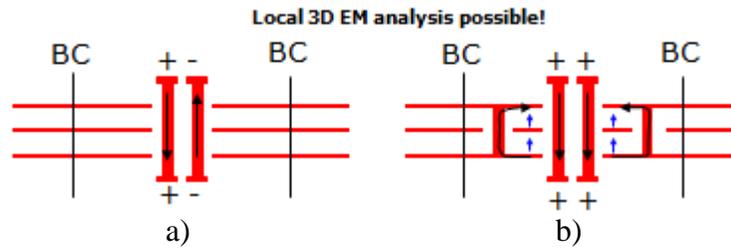


Fig. 2. Localization of the differential mode a) and common mode b) of differential via-holes. Differential mode in the electrically close vias does not require stitching vias. BC – lines for possible boundaries for analysis.

If stitching vias are not used to localize the common mode, simulation of the whole board in a 3D full-wave solver with all plane terminations may be required. As in the case of single-ended vias, it is hardly ever possible and not practical. Use of a hybrid solver with 2D transmission plane models is practical, but accurate only if such solvers include 3D full-wave models for differential mode. On the other hand, accurate analysis of the differential vias with common mode may be not required if common mode is relatively small by design [1].

S-parameters

Scattering parameters is a natural black-box description of a linear system in the frequency domain. The system can be smaller, comparable with, or larger than wavelength. **All types of via-holes and complete interconnect part of a data channel can be accurately characterized with S-parameters.** For serial channel analysis, S-parameters of via-holes and other components are usually concatenated and simulated either in frequency or in time domain with models of drivers and receivers. S-parameters can be computed with an electromagnetic simulator or measured with a Vector Network Analyzers (VNA) or by post-processing TDR/TDT responses (less accurate but may be acceptable for analysis of serial channels). **Thus, S-parameters is the best choice for precise validation of interconnect models.** S-parameters of a N-port structure is N by N matrix (2

by 2 for 2-port single ended channel). Each element of the S-matrix $S_{i,j} = \frac{b_i}{a_j}$

either reflected from or transmitted through the structure to the incident wave a_j . The waves are defined as a simple but very important transformations through voltage and current at a port i :

$$a_i = \frac{1}{2\sqrt{Z_0}}(V_i + Z_0 \cdot I_i), \quad b_i = \frac{1}{2\sqrt{Z_0}}(V_i - Z_0 \cdot I_i),$$

where Z_0 is the normalization impedance (usually

50 Ohm). All elements of S-matrix are complex numbers with magnitude ranging from 0 to 1 for passive structures. **Diagonal elements of S-matrix characterize the reflection from the structure.** All elements of a channel including vias must be designed to have minimal reflection over the frequency band of interest (minimum of differential mode reflection for differential via-holes). **Off-diagonal elements are either useful transmission coefficients or non-desirable coupling or transformation coefficients.** Ideal loss-less interconnect has transmission coefficient 1. All elements of S-matrix are unit-less, but they can be expressed in dB as $|S_{i,j}|_{dB} = 20 \cdot \log(|S_{i,j}|)$. **Minus infinity dB corresponds to ideal non-reflective structure. Everything above it is the reflection loss. 0 dB corresponds to the ideal transmission through the structure. Everything below it is the transmission loss.**

Modeling via-holes

There are no simple via-hole models in microwave frequency range for analysis of multi-gigabit signal propagation (especially if vias are going through multiple parallel planes).

Electromagnetic analysis is usually required. We can distinguish three different approaches – distributed LC models, models with transmission planes, and 3D full-wave models.

Distributed LC models with ladder-type connections of capacitances and inductances [2, 5] are similar to a lumped LC model of a transmission line. It works well for localized via-holes at lower data rate or slow edges (signal spectrum up to 1-3 GHz). L and C values can be calculated with a static and magneto-static solver or with the infinite radial waveguide or parallel-plane models.

Transmission plane models – impedance of power distribution parallel planes is computed to simulate current return path [3]-[6]. Good for non-localizable cases for signals with spectrum up to 3 GHz (may be extended by hybridization with 3D models). Parallel-plane structures have low impedance by design at these frequencies and even simplified models are sufficient to predict behavior of vias. Both distributed LC and transmission plane models usually ignore the non-circular shapes of anti-pads (oblong or rectangular) and do not account for the transition from the trace to via-holes. That is why they may be considered as the first approximation only for a serial channel analysis.

3D full-wave electromagnetic analysis is a solution of Maxwell's equations in 3D space with all field components and displacement term included. Transition from transmission lines to vias and geometry of pads and anti-pads are usually included in such analysis. Overview of the different methods can be found in [5]. Signal and the return paths currents have to be confined into small area electrically isolated from the rest of the board. Geometry of the via-hole barrel, pads and anti-pads can be adjusted to minimize the signal reflection over the frequency band of interest. There are many electromagnetic solvers on the market that can handle such localizable cases - Simbeor 2008 [7] is used here to generate examples. **Analysis of non-localized structures with a 3D full-wave solver may require geometry of the whole board and is usually not practical,** because of extremely long simulation times and no possibility to re-use the same via at different locations on the board.

Designing localized vias

Three structures are used here as examples. They were designed with Simbeor 2008 software [7] and investigated experimentally by Teraspeed Consulting Group (www.teraspeed.com). Frequency-dependent dielectric properties for all cases were extracted with methodology described in [8].

The first structure is a micro-strip channel with 6 single-ended via-holes without stitching vias as shown in Fig. 3. The via-holes are not localized (change of reference planes and no stitching vias nearby) and thus, cannot be simulated in isolation from the rest of the board. But if we do such analysis, we can observe good correspondence of the transmission and reflection at frequencies up to 3 GHz as shown in Fig. 4. This is because of the low impedance for the current return path provided by the parallel planes and by some remote stitching vias at low frequencies. Resonant properties of the board show up at higher frequencies and the whole board has to be simulated to predict behavior of the vias.

The second structure is the same micro-strip channel, but each signal via-holes is isolated with four stitching vias as shown in Fig. 5. The stitching vias minimize the impedance of the return path up to 20 GHz and allow local electromagnetic analysis. The via-hole geometry has been optimized to have minimal reflection. The reflection from the actual via-hole on the board was larger than predicted probably due to either manufacturing tolerances or weave effect. Though the final via geometry is relatively close to optimal and acceptable for practical 6-10 Gb/s data channels as follows from the transmission coefficient magnitude and phase plotted in Fig. 6.

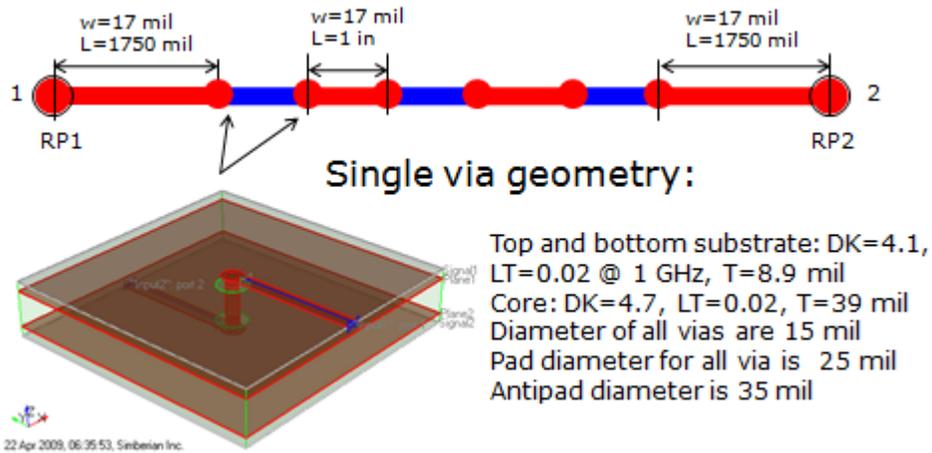


Fig. 3. Micro-strip channel with 6 via-holes without stitching vias (not localizable case).

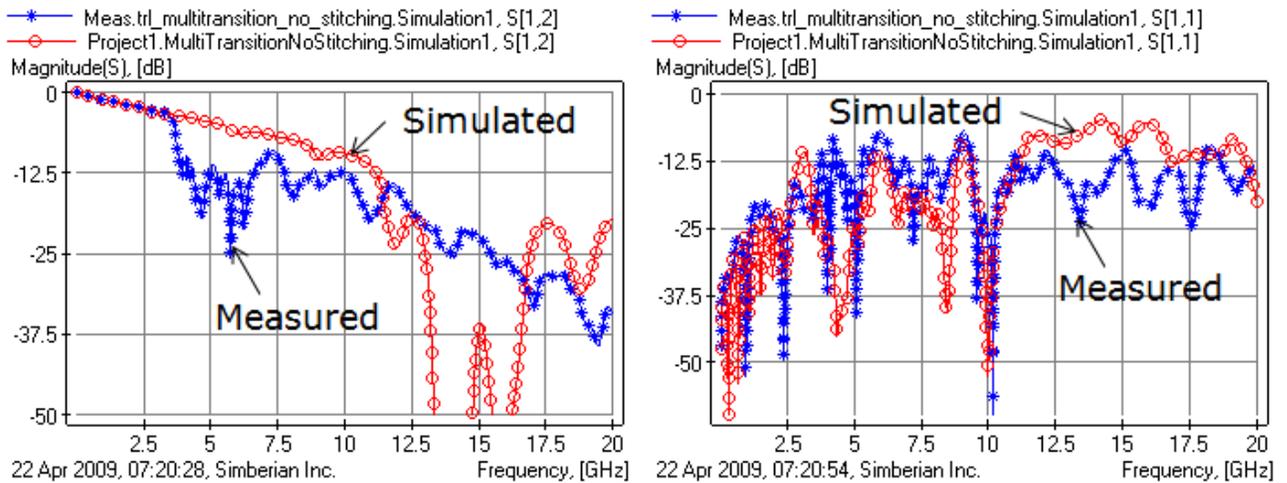


Fig 4. Magnitude of the transmission coefficient $S[1,2]$ (left graph) and reflection coefficient $S[1,1]$ (right graph) for the channel without stitching vias. Accuracy is not acceptable above 3 GHz for multi-gigabit channels due to the lack of current return path localization.

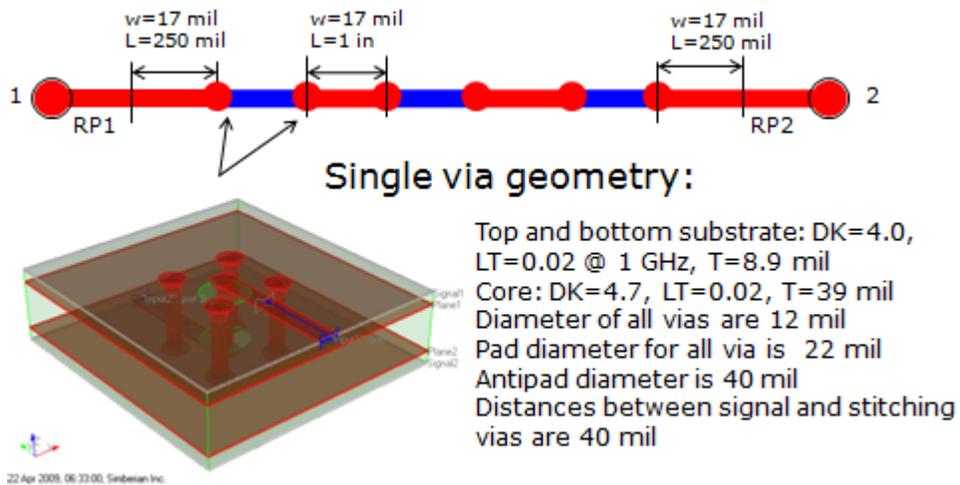


Fig. 5. Micro-strip channel with 6 vias with stitching vias (localizable case). Reference planes are shifter to planes RP1 and RP2 during de-embedding.

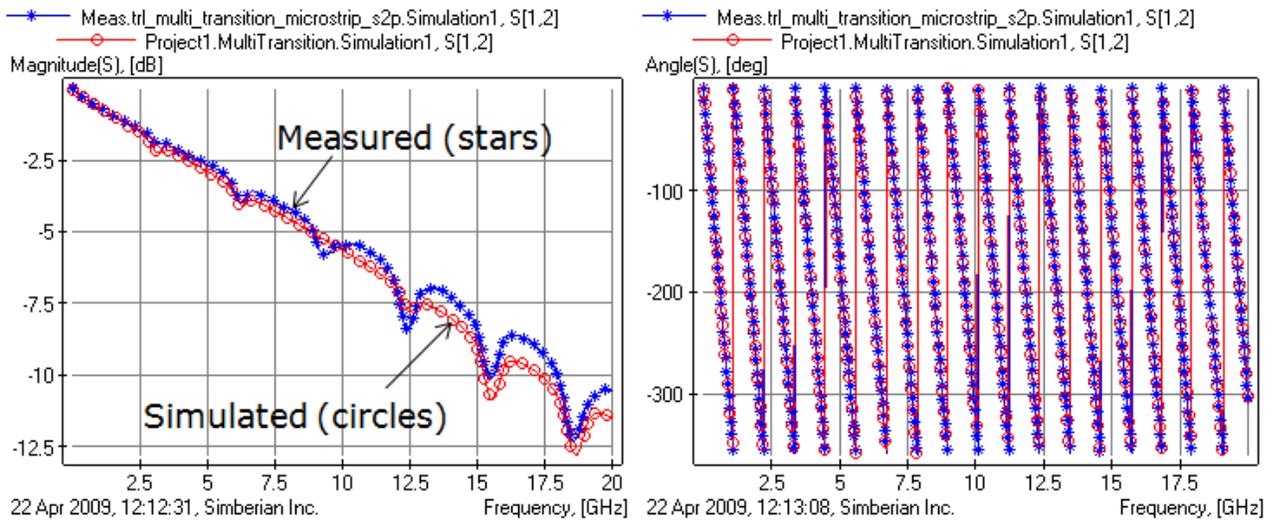


Fig. 6. Magnitude (left graph) and phase (right graph) of the transmission coefficient S[1,2]. The accuracy of analysis with localized via-holes is acceptable for 10 Gb/s channel design.

The final structure is differential transmission line with differential via-holes shown in Fig. 7. As in the case of single-ended via-hole with stitching vias, the geometry of the differential vias has been synthesized with Simbeor 2008 software to minimize the reflection of the differential mode. Four stitching via-holes are used around the differential via-holes to localize the common mode. The final via-holes are acceptable for 6-10 Gb/s transmission and the model shows good agreement with the measured data as shown in Fig. 8. Correspondence in the common mode transmission and reflection was also acceptable due to use of the stitching vias.

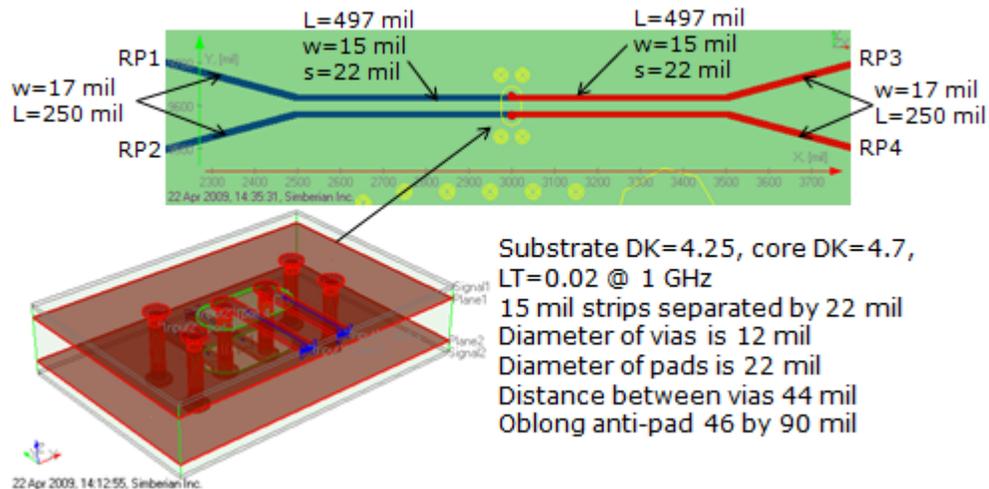


Fig. 7. Differential micro-strip lines with minimal-reflection differential via-holes.

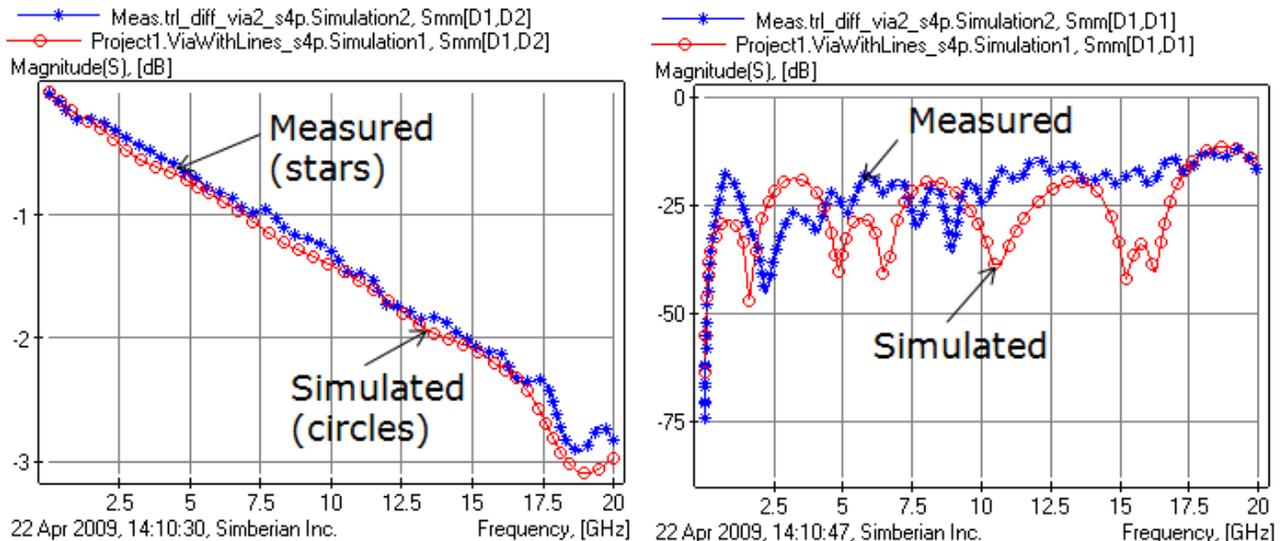


Fig. 8. Differential mode transmission (left graph) and reflection (right graph) coefficients of differential micro-strip line with differential via-holes.

Conclusion

It was shown that all via-holes can be classified as localizable and non-localizable. **Only localizable via-holes can be reliably simulated with a 3D full-wave solver in isolation from the rest of the board and safely used in multi-gigabit serial data channels.** On the other hand, non-localizable via-holes may require board-level analysis with all power distribution structures included. Reliable analysis of non-localizable vias at microwave frequencies is practically impossible task and such vias should be avoided by design. Single ended via-holes can be localized with electrically close stitching vias connecting all reference planes of the connected transmission lines. Differential via-holes are localizable for differential mode only if the barrels are electrically close. Common mode of differential via-holes can be localized with the stitching vias similar to the single-ended vias. In addition to the localization, the via-hole geometry has to be optimized to have minimal reflection loss over all frequency band of interest to minimize the effect of resonances created by reflections between via-holes. **It was demonstrated that localizable minimal-reflection single-ended and differential via-holes can be successfully designed for 6-10 Gb/s channels with good correspondence of simulations with measurements.**

Simbeor solutions used in this paper are available at

www.simberian.com/AppNotes/Solutions/DesigningLocalizableMinimalReflectionVias_2009_05.zip

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Glossary and definitions

Micro-strip line – trace over a conductive plane on the surface of a board.

Strip-line – trace in the internal layer of a board shielded by two conductive planes in adjacent layers.

Reference plane – large conductive area near a trace that defines properties of the wave propagating in the trace (characteristic impedance and propagation constant). Planes above, below or next to a strip line are the reference planes. Micro-strip lines usually have one reference plane and strip lines always have at least two reference planes. Coplanar lines may have up to 4 reference planes.

Single-ended line – one trace with one or more reference planes.

Differential line – two traces with one or more reference conductors. The structure supports two propagating waves or modes – differential or odd to transmit the signal and common or even that is not useful and has to be suppressed.

Via-hole or PTH - connection between different layers on multilayered PCB or package.

Signal via-hole – via-hole connecting two or more signal traces in different layers.

Stitching via - via-hole connecting reference planes of the transmission lines. Typically, for multi-gigabit applications, all reference planes of the connected traces have to be connected with the stitching vias.

Via-hole stub is a segment of a via-hole outside of the connected signal layers (increases the reflection loss and causes resonances degrading the signal).

Via-hole barrel – conductor-plated cylinder with diameter equal to the drill diameter of via-hole (distance between the barrels mostly defines the effective inductance).

Via-hole pad – small planar metalized area around the barrel connected to the barrel (defines effective capacitance of a via segment).

Via-hole anti-pad – clearance between pad and conductive area in the same layer (defines effective capacitance of a via segment).

Frequency range of interest for analysis and measurement is defined by the spectrum of the signal. For practical applications, it can be defined as fourth or fifth harmonic of a periodic pulse train (about 20-25 GHz for 10 Gbps signal) or the knee frequency equal to $0.5/T_r$, where T_r is expected rise time of the signal (with 20 ps rise time, it is 25 GHz). Structures on the board can be characterized as **electrically close** if distance between them is a small portion of the wavelength at the maximal frequency of interest (one-tenth of the wavelength in dielectric or smaller for instance).