

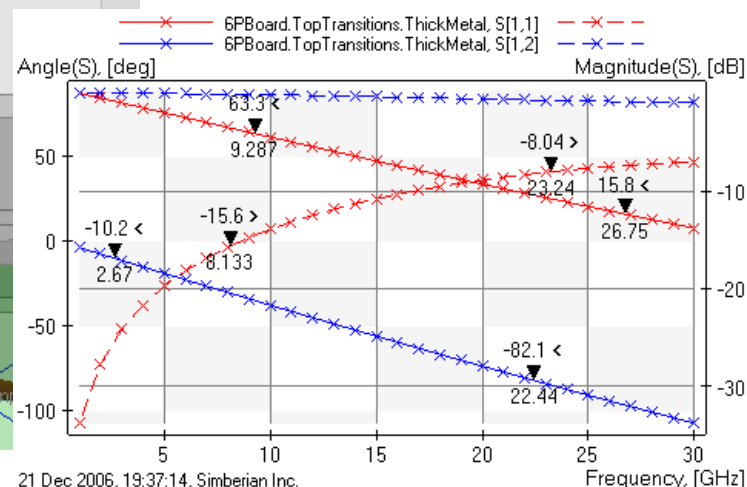
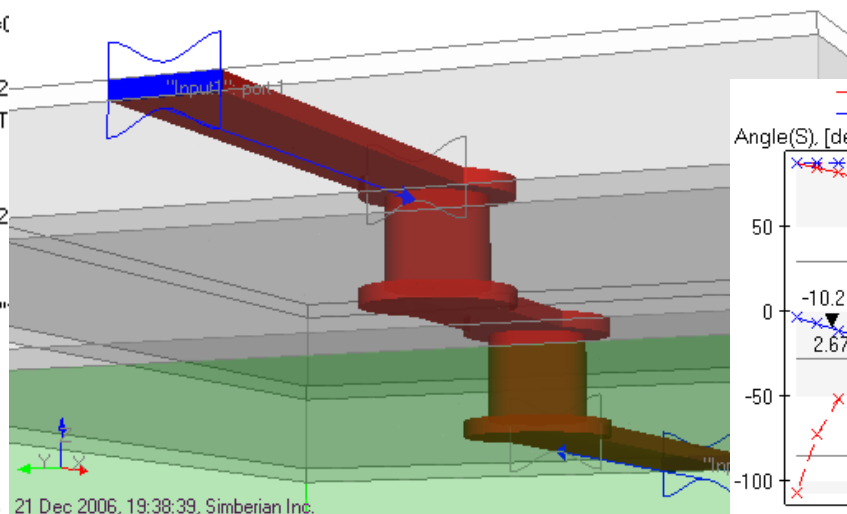
# Minimization of Reflection from AC Coupling Capacitors

Solution: "MicroVias"

- 6PBoard
  - Materials
    - "copper", RRes=1, Rough=0.01
    - "IdealMetal"
    - "prepreg", DK=4.7, LT=C
    - "Vacuum"
    - "FR4", DK=4.2, LT=0.02
  - StackUp: LU=[mil], NL=15, T
  - TopTransitions
    - CircuitData: LU=[mil]
    - Multiport: 2 inputs, 2
    - LatticeBox
    - Geometry
      - GeoComposite: "
      - TLines
      - Inputs
    - ThickMetal
    - CollapsedMetal
  - BottomTransition
- Graph1(MultiportParameters vs. 21 Dec 2006, 19:38:39, Simberian Inc.)
- Graph2(MultiportParameters vs. Frequency)

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# Overview

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- Introduction
- De-compositional analysis of a channel with AC decoupling capacitors
- Building models for AC capacitor mounting structures for a single-ended channel
- Minimization of reflection from the mounting structures with cut-outs in the reference plane
- Analysis of simple channels with AC coupling capacitors
- Conclusion

# Introduction

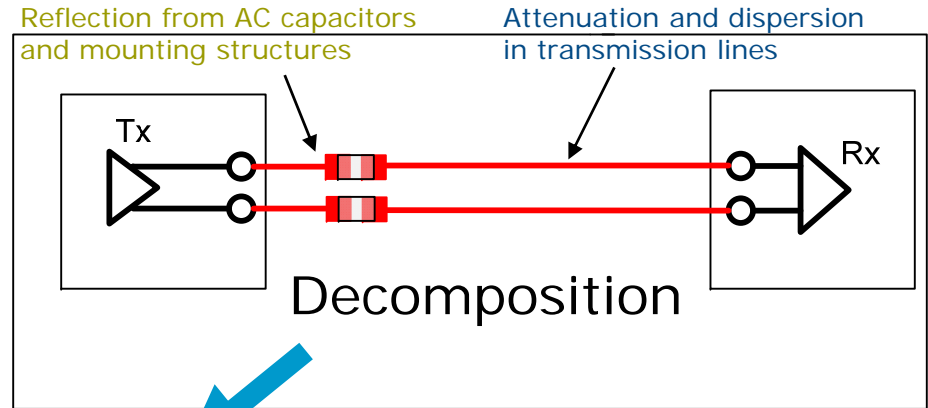
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- Serial multi-gigabit data channels usually have capacitors connected in series in micro-strip lines (AC coupling capacitors) to pass through the high-frequency signals content and to allow different DC supply for a driver and receiver at the same time
  - Mounting structures of such capacitor and capacitors themselves are discontinuities and reflection from them have to be minimized to improve signal quality
  - 3D electromagnetic analysis is required to estimate and to minimize the reflection from the AC coupling capacitors and mounting structures
- This example is follow-up to App Note #2008\_02
  - Demonstrates how to minimize reflection from the AC coupling capacitors using cut-outs in the reference plane
  - Demonstrates how to build a system-level model of a simple channel with AC coupling capacitors within Simbeor environment
- Simbeor 2008 built on August 25<sup>th</sup> 2008 is used to generate the results

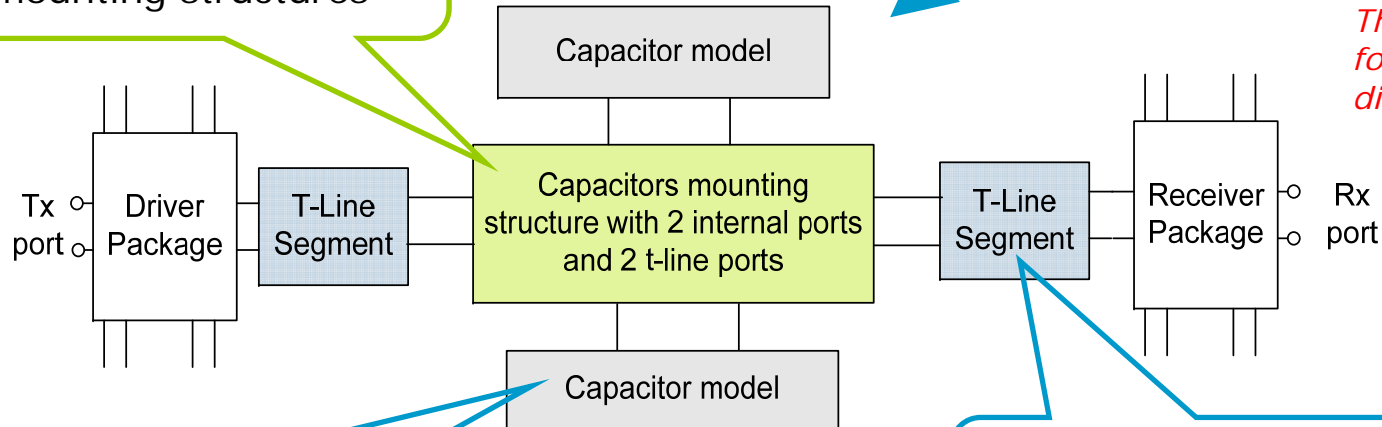
# De-compositional analysis of a serial multi-gigabit channel with AC coupling capacitors

*3-D full-wave electromagnetic analysis is required to generate models both for the mounting structure and transmission lines!*

*We will use Simbeor to do it.*



Multiport S-parameter model for the capacitors mounting structures



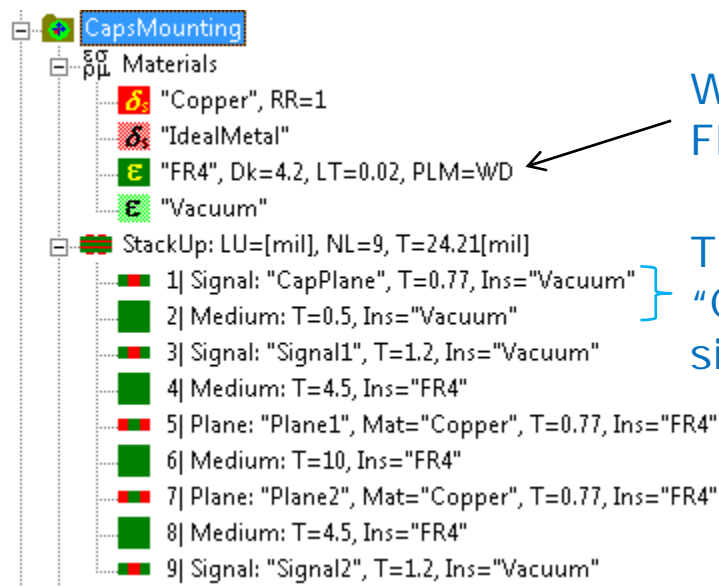
*The same approach for single and differential channels*

Capacitor model from a manufacturer (circuits or S-parameters)

W-element models for t-line segments defined with RLGC(f) p.u.l. tables

# Materials and stack-up for analysis of the capacitors mounting structures

- ❑ Solution Simbeor Solutions/ PCB\_MCM/ AC\_CouplingCaps/ AC\_CouplingCaps.esx created for this investigation
- ❑ Simple 4-layer stackup with two signal layers and two plane layers
- ❑ Stackup is extended to simulate connection of the capacitor slightly above the board surface



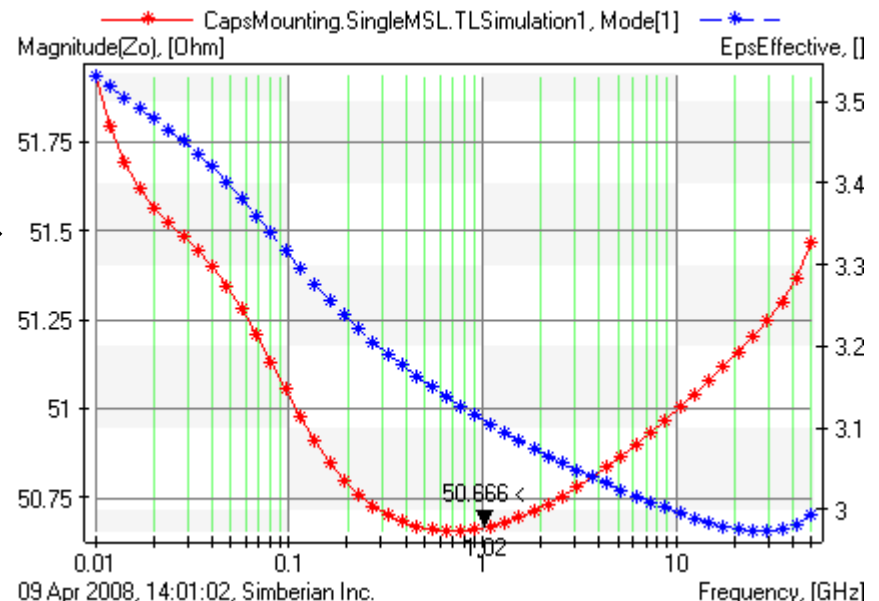
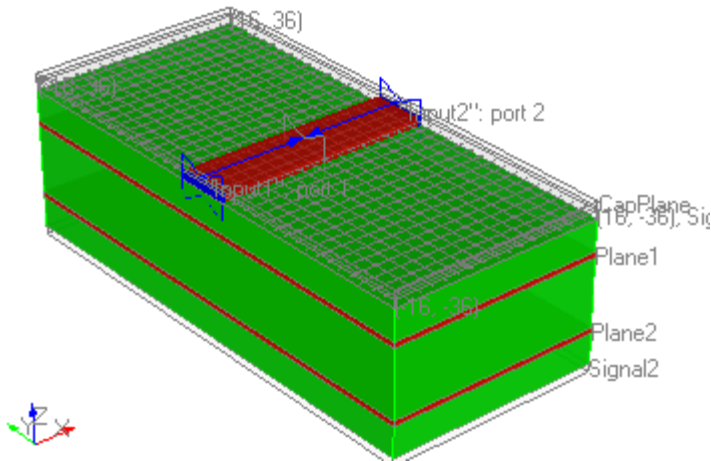
Wideband Debye model for FR-4 type dielectric

Thin layer of air and additional layer "CapPlane" of signal-type are added to simulate non-flat connection of the capacitors

*Use Help > Tutorials > Tutorial 1 to learn how to build models for materials and stackup*

# Single-ended channel – transmission line (circuit SingleMSL)

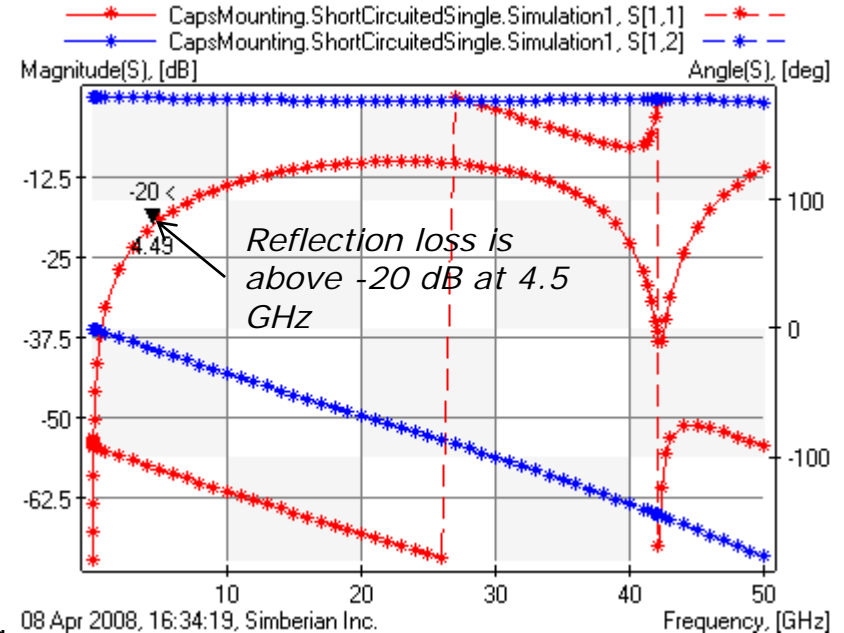
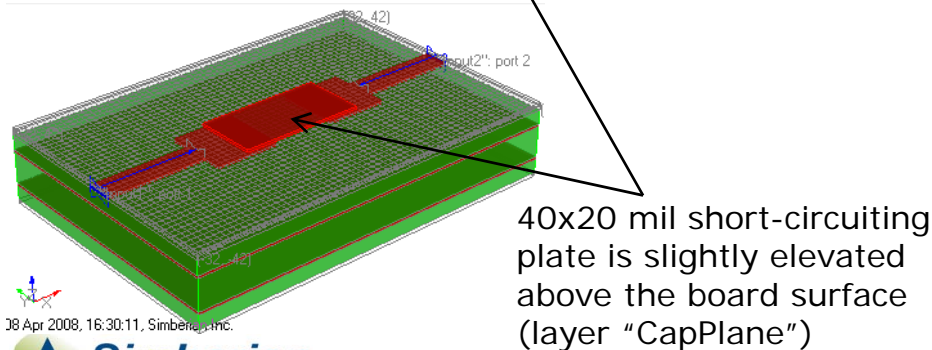
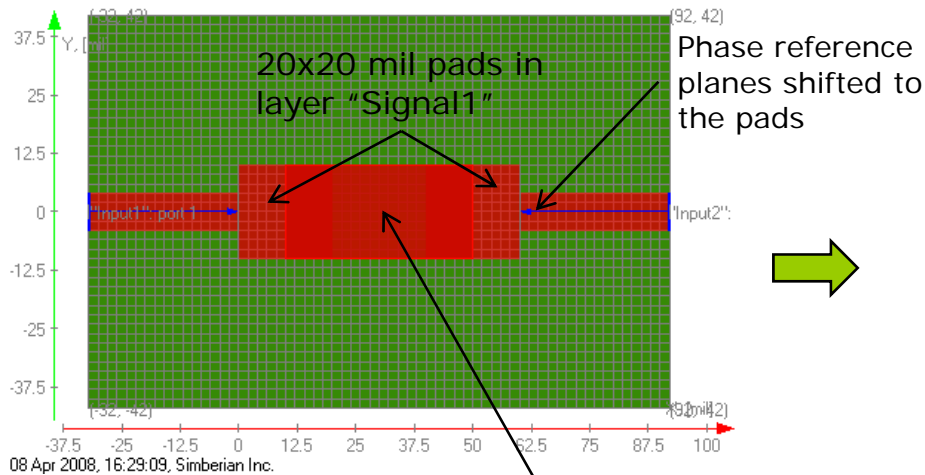
- 8 mil wide strip on 4.5 mil substrate with  $Dk=4.2$ ,  $LT=0.02$  at 1 GHz and wideband Debye dielectric model



*Use Help > Tutorials > Tutorial 2 to learn how to build broadband RLGC(f) models for transmission line*

# Short-circuit experiment with 0402 capacitor footprint (SCSingle)

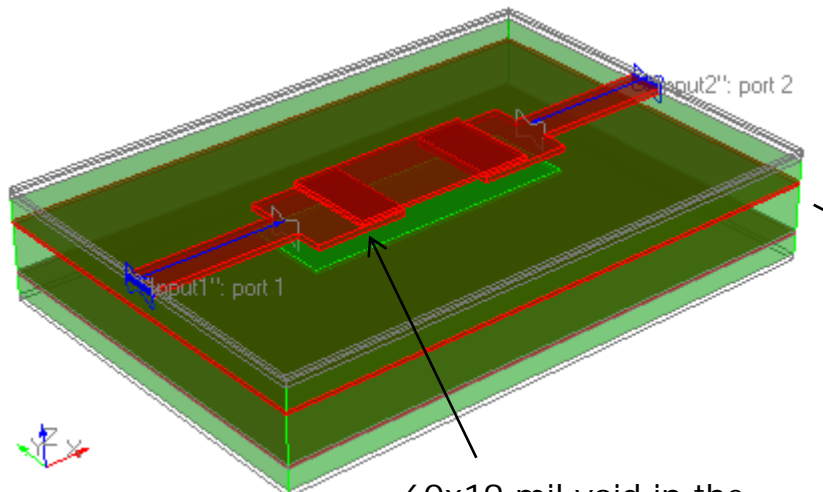
- Capacitor in micro-strip line with 8 mil wide trace
- Allows us to estimate the minimal possible reflection
- May be used to do the through calibration of the internal ports





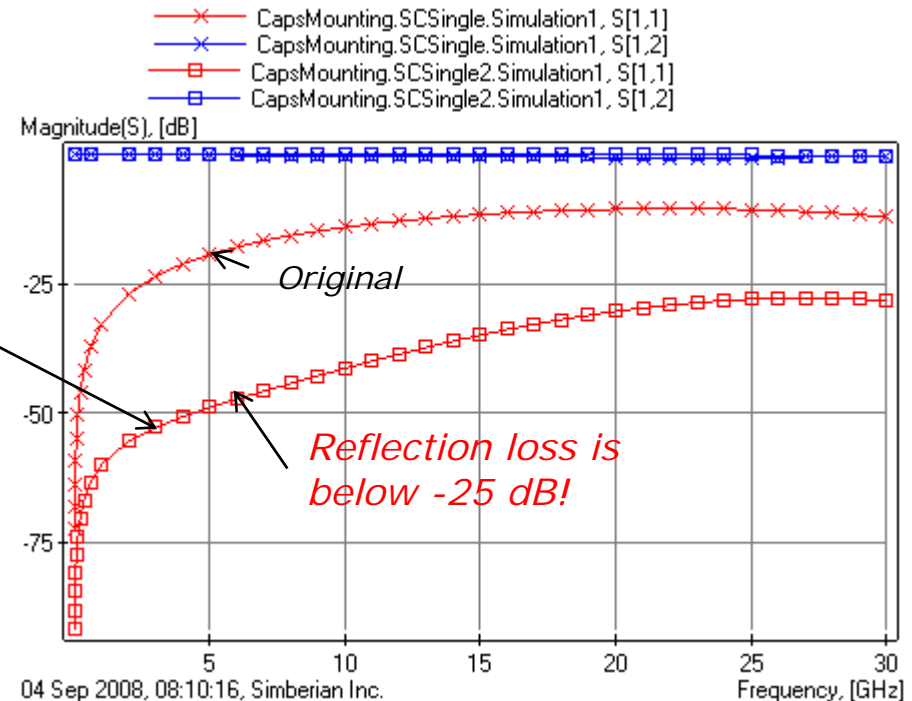
# Short-circuit experiment with 0402 capacitor footprint with cut-out (SCSingle2)

- Cut-out 60 mil by 19 mil in the reference plane reduces the reflection loss



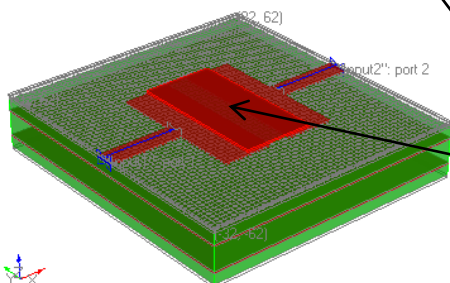
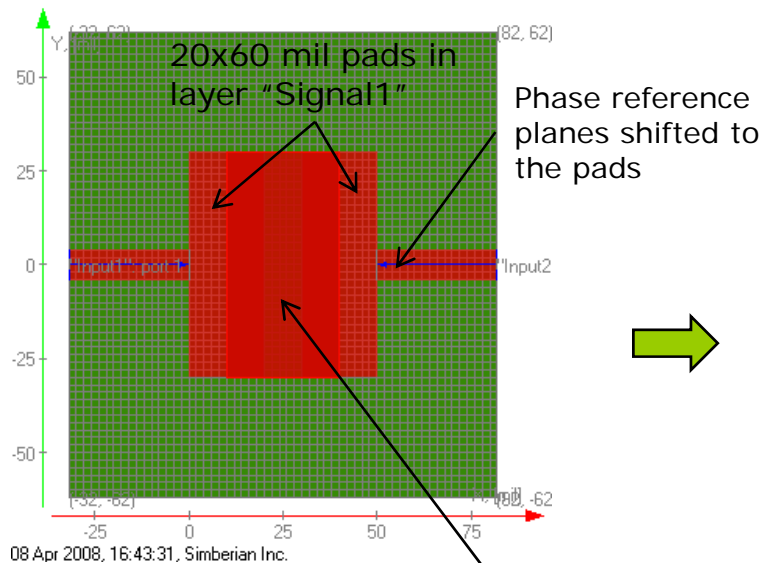
04 Sep 2008, 08:03:18, Simberian Inc.

60x19 mil void in the reference plane below the capacitor mounting structure



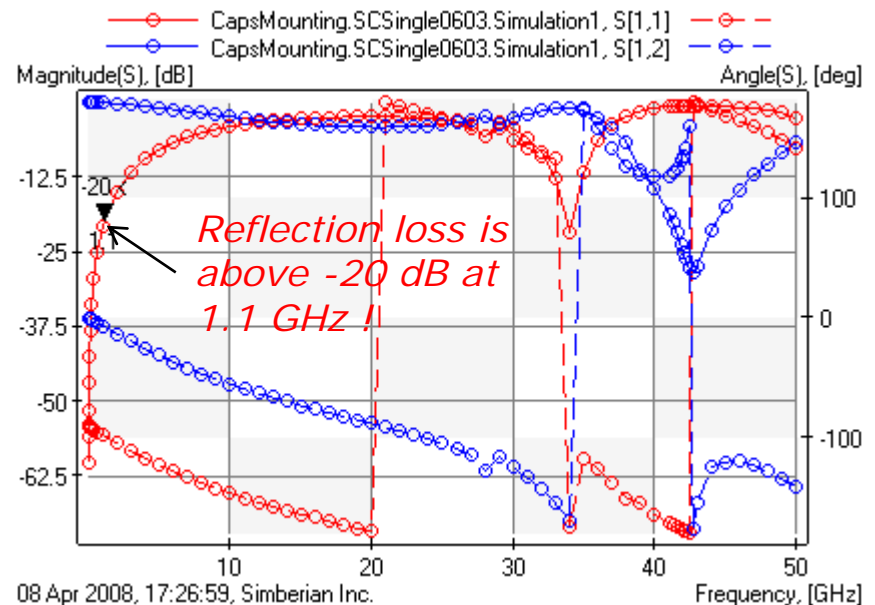
# Short-circuit experiment with 0603 capacitor footprint (SCSingle0603)

- The larger the footprint the larger the minimal possible reflection loss
- Impedance of the actual capacitor will make reflection worse



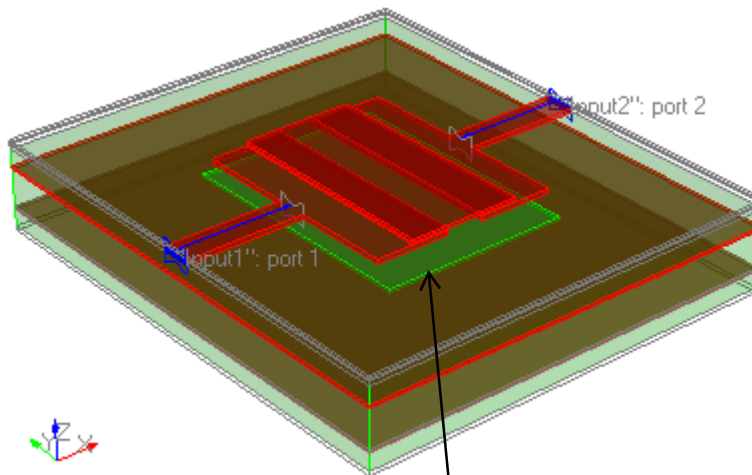
30x60 mil short-circuiting plate is slightly elevated above the board surface (layer "CapPlane")

Simulation from 10 MHz to 50 GHz

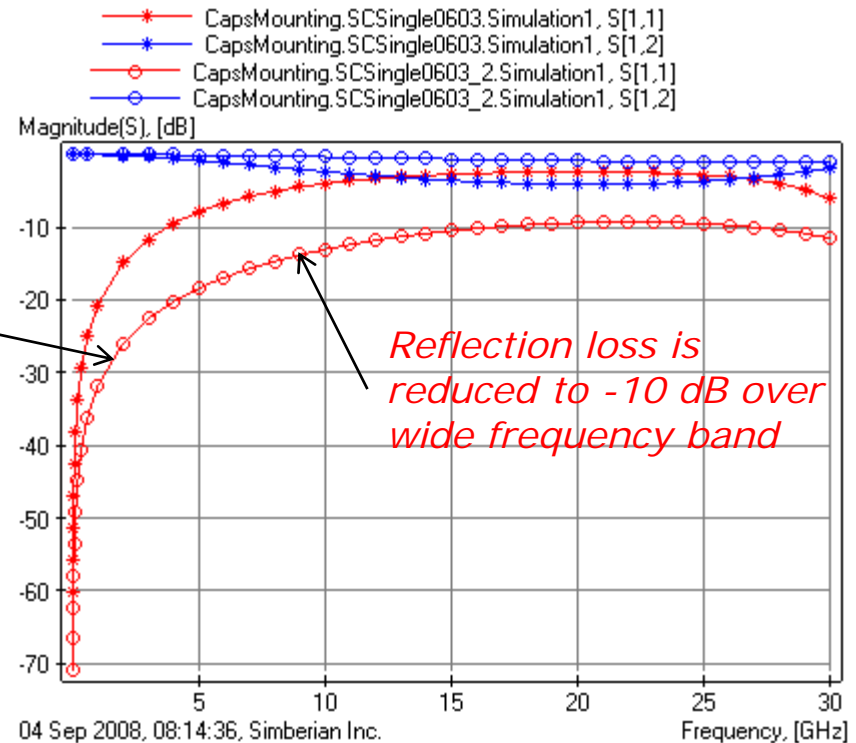


# Short-circuit experiment with 0603 capacitor footprint with cut-out (SCSingle0603\_2)

- Cut-out 50 mil by 68 mil in the reference plane considerably reduces the reflection loss

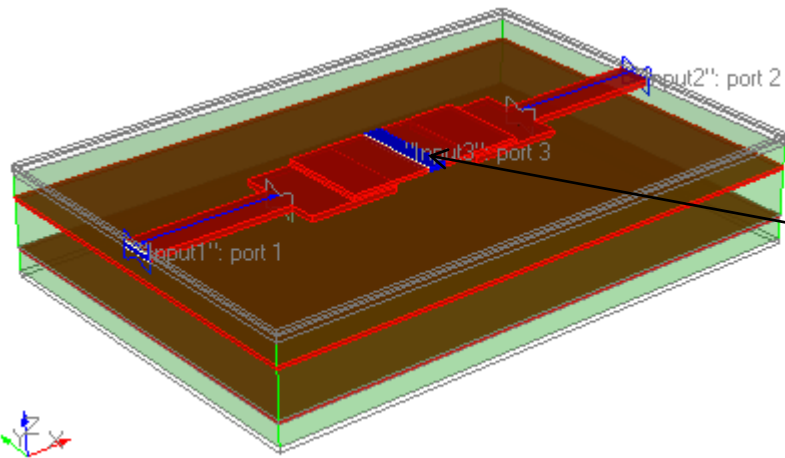


50x68 mil void in the reference plane below the capacitor mounting structure



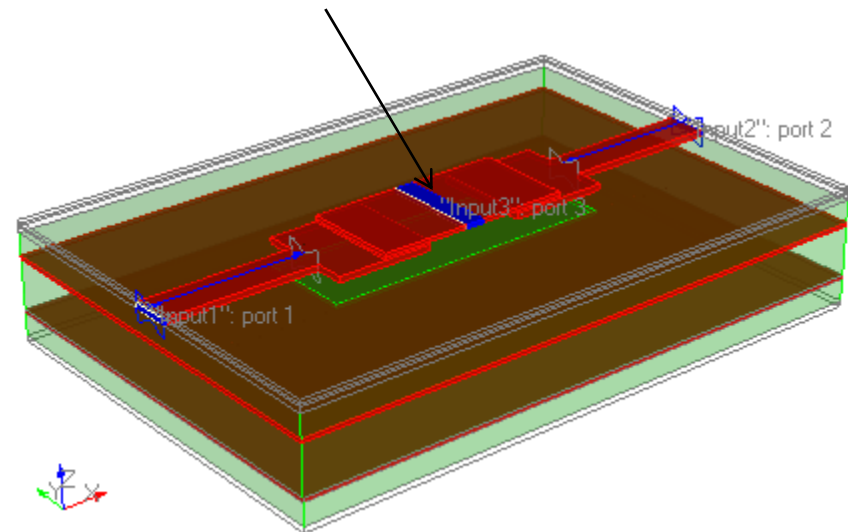
# Series internal port to connect 0402 capacitor (SPSingle and SPSingle2)

- Series port is the only option in case of cut-out of the reference plane below the capacitor (no reference below the pads to construct parallel ports)



3-port broad-band S-parameter models of the mounting structures are extracted for both configurations

Series X-directed port #3 to connect the capacitor model

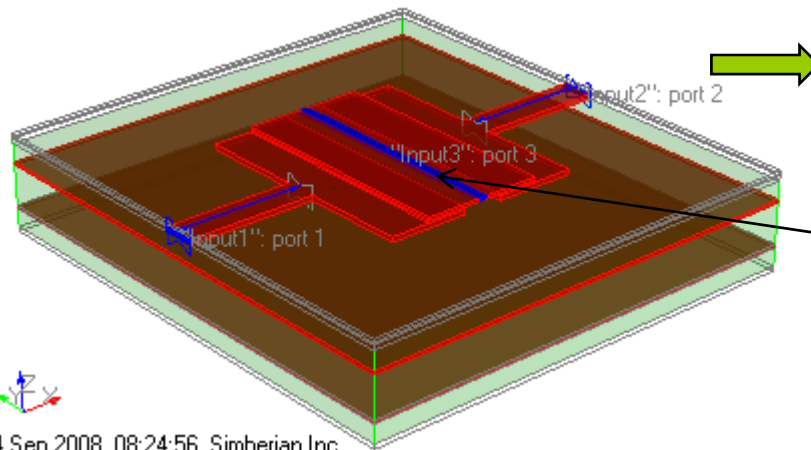


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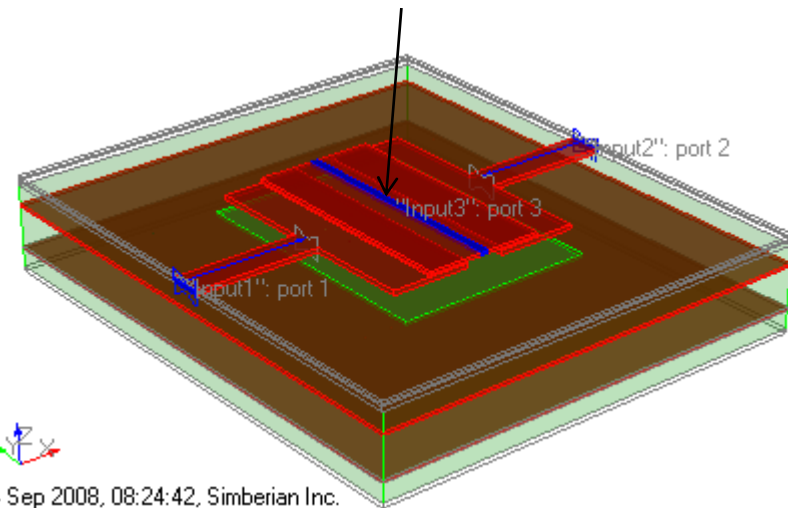
# Series internal port to connect 0603 capacitor (SPSingle0603 and SPSingle0603\_2)

- Series port is the only option in case of cut-out of the reference plane below the capacitor (no reference below the pads to construct parallel ports)



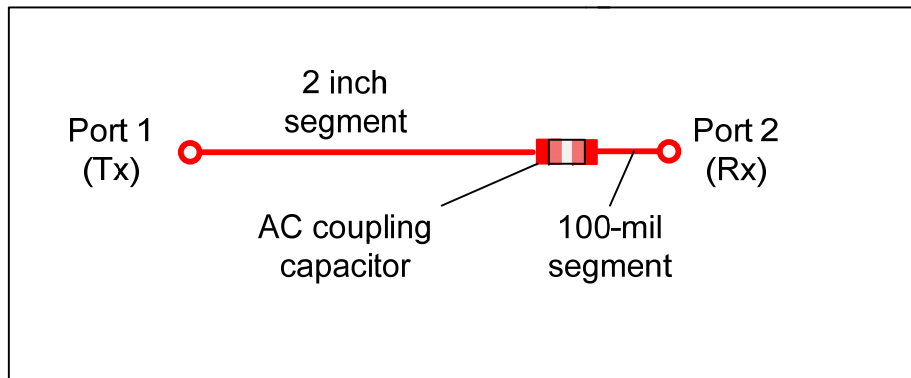
3-port broad-band S-parameter models of the mounting structures are extracted for both configurations

Series X-directed port #3 to connect the capacitor model



# Analysis of a simple data channel with AC coupling capacitor (circuits in the project Channels)

- Capacitor model:  $C=100$  nF,  $ESR=1$  mOhm,  $ESL= 100$  nH
- Capacitor is placed closer to the receiver port 2

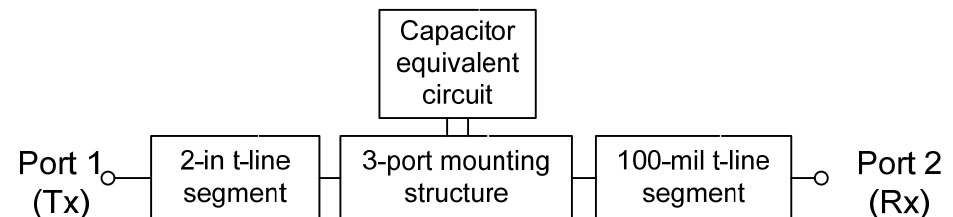


← Sketch of the channel

We will use broadband RLGC(f) model of 50-Ohm micro-strip line and extracted S-parameters of the capacitor mounting structure

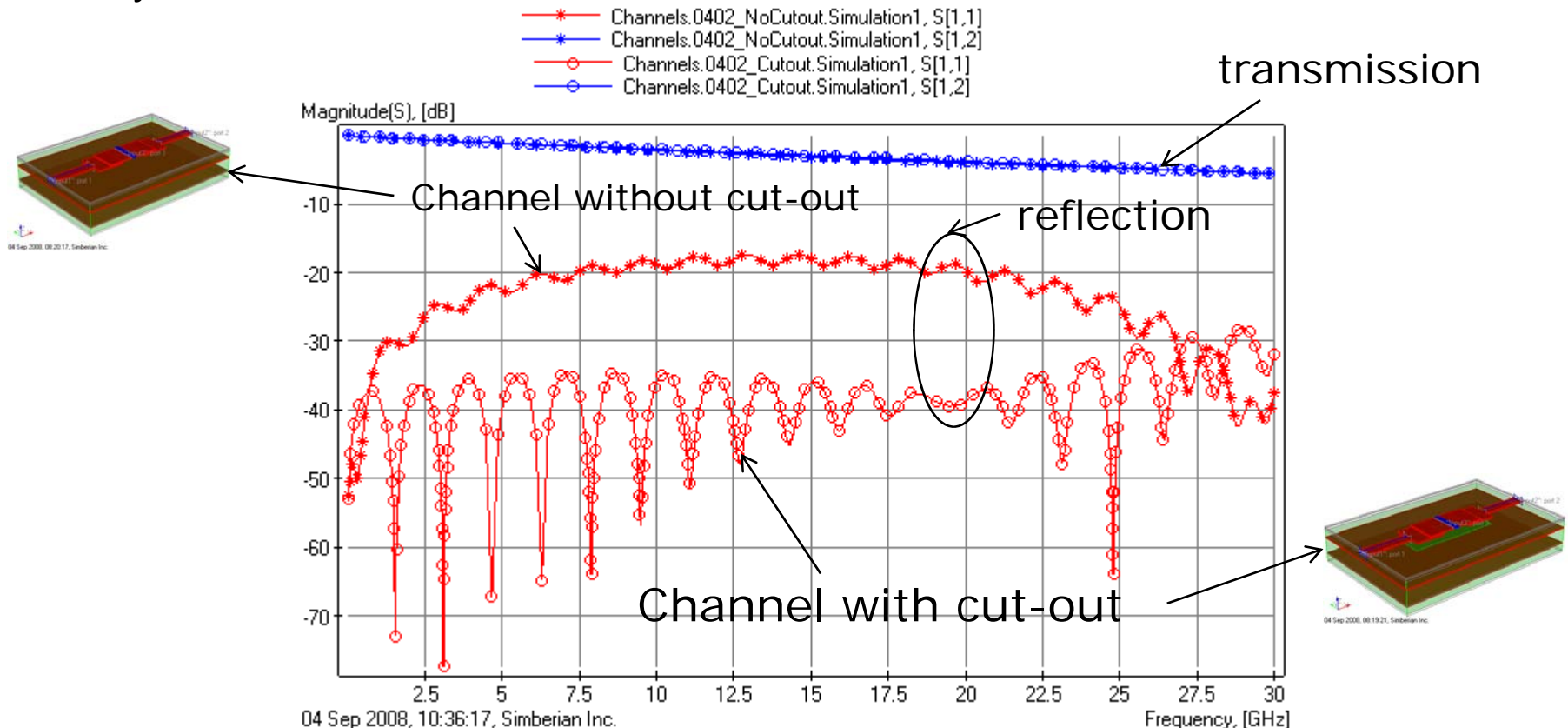
Simbeor de-compositional model of the channel

The channel is simulated in frequency domain as connection of multiports



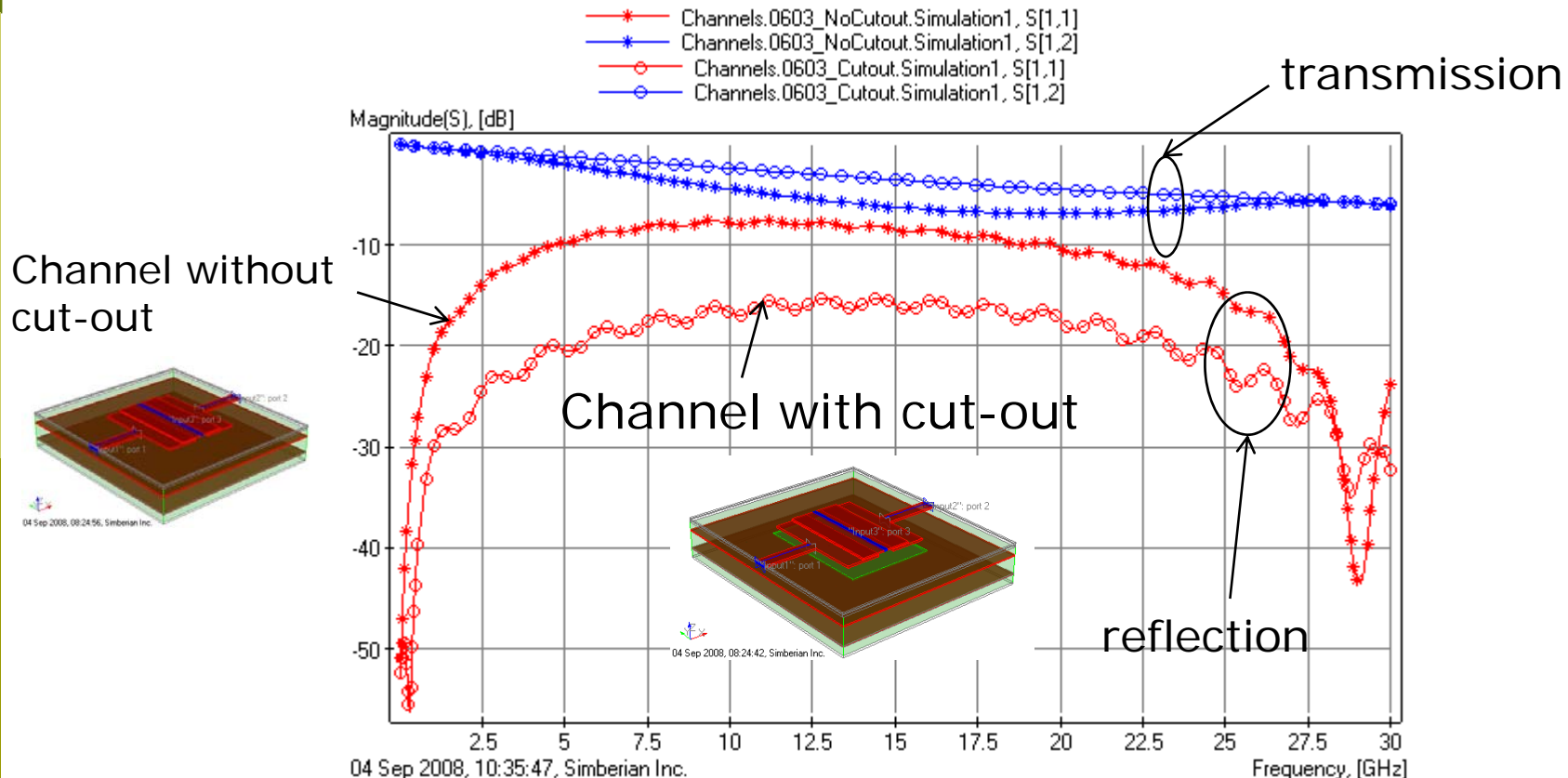
# Simbeor models of the simple channel with 0402 capacitor

- We can see considerable reduction of the channel reflection loss
- S-parameter model of the complete channel can be used in a system-level simulator



# Simbeor models of the simple channel with 0603 capacitor

- Considerable reduction of losses in the channel can be observed
- Without cut out a similar channel with additional via-hole discontinuities may fail because of resonances between the mounting structure and via-holes





# Conclusion

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- ❑ Simple examples of Simbeor application for extraction of electromagnetic models and for minimization of reflection losses from AC coupling capacitors are provided
- ❑ Optimal geometry of the mounting structure practically removes reflections from 0402 capacitors and considerably reduces the reflection loss from 0603 capacitors
- ❑ Electromagnetic models of the mounting structures can be used
  - For accurate modeling of multi-gigabit serial data channels
  - For identification of the models for the capacitors by comparison of simulation and measurement results
- ❑ Model of a complete channel in frequency domain is convenient to estimate insertion and reflection losses and can be used as a black-box model in a system-level simulator
- ❑ Analysis and loss minimization for differential channels is similar
- ❑ Setting up all simulations and model building with Simbeor took approximately 1 hour

# Solutions and contact

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- Simbeor solution file is in  
Simbeor Solutions/ PCB\_MCM/ AC\_CouplingCaps/  
AC\_CouplingCaps.esx
  - It contains all electromagnetic models and linear circuit analysis
- Send questions and comments to
  - General: [info@simberian.com](mailto:info@simberian.com)
  - Sales: [sales@simberian.com](mailto:sales@simberian.com)
  - Support: [support@simberian.com](mailto:support@simberian.com)
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